

8	7
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HSF Property:ROHS or Halogen-Free(5L3?)

# DAKAR10F/FG

2011.09.02

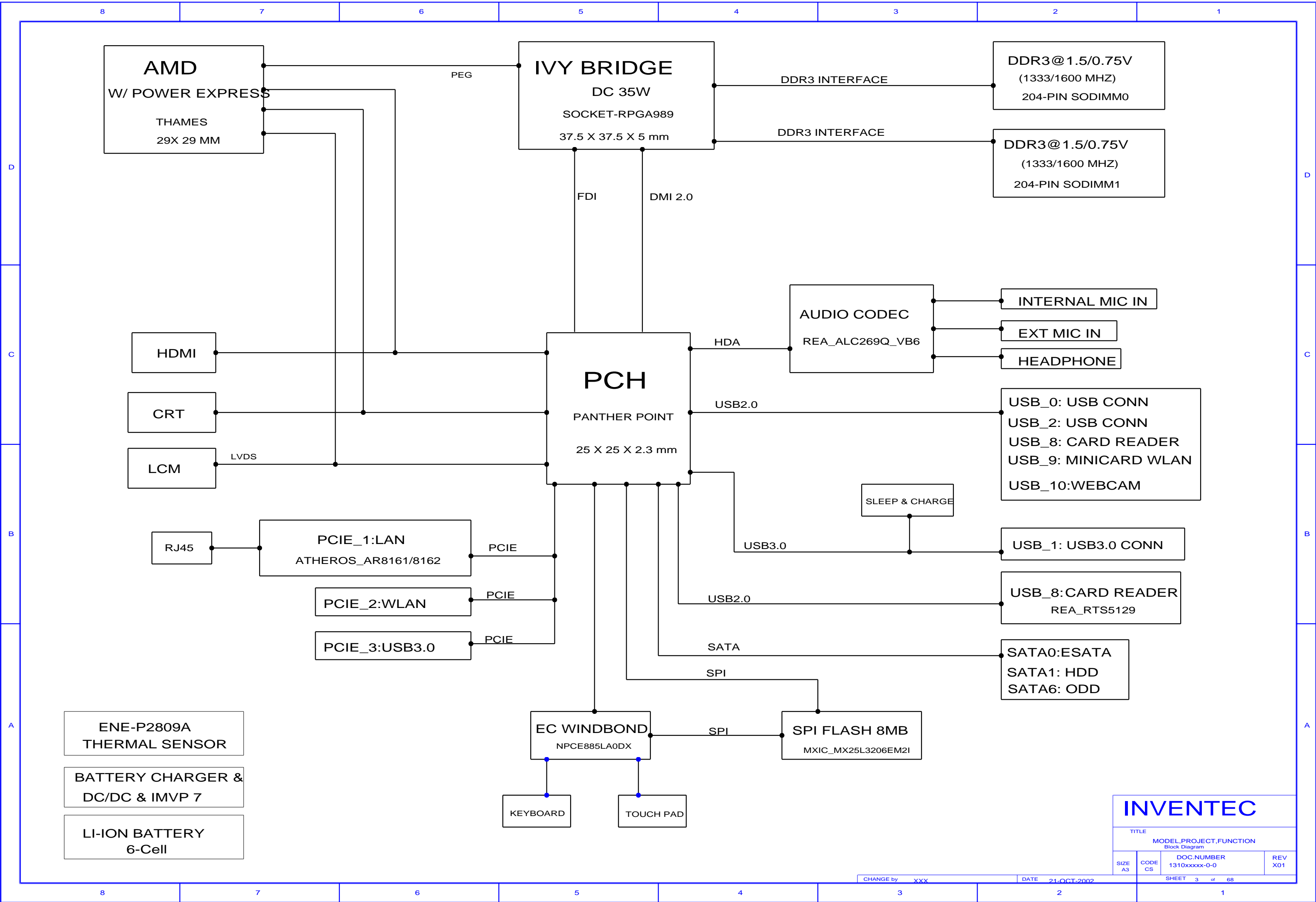
21-OCT-2002		
DATE	CHANGE NO.	REV

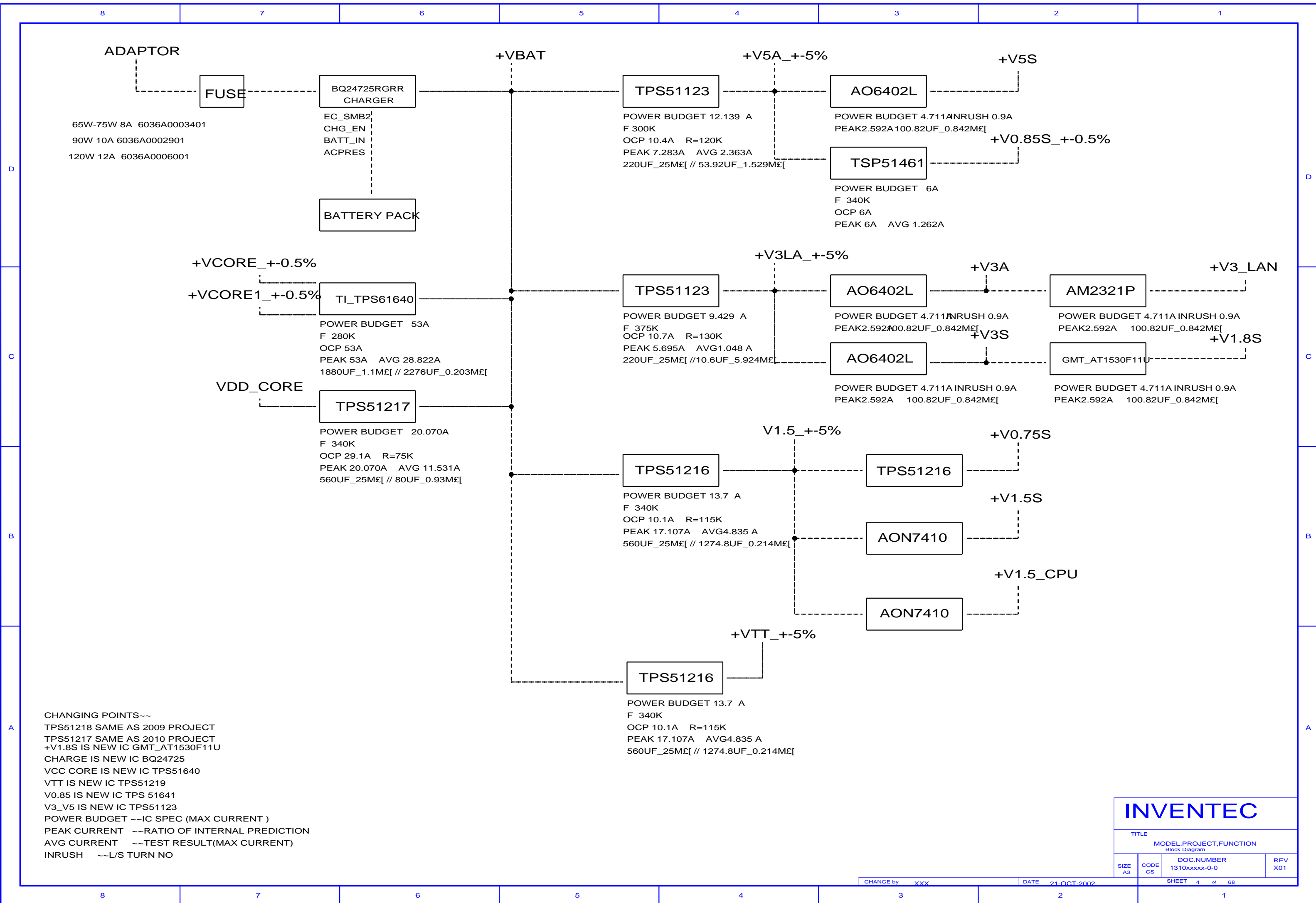
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DESIGN									
CHECK									
RESPONSIBLE									
SIZE=			VER:			TITLE <b>MODEL,PROJECT,FUNCTION</b> <b>Everest Main Board</b>			
FILE NAME:						SIZE C	CODE CS	DOC.NUMBER	REV X01
P/N	XXX	1310xxxxx-0-0				SHEET                      1                      of                      68			

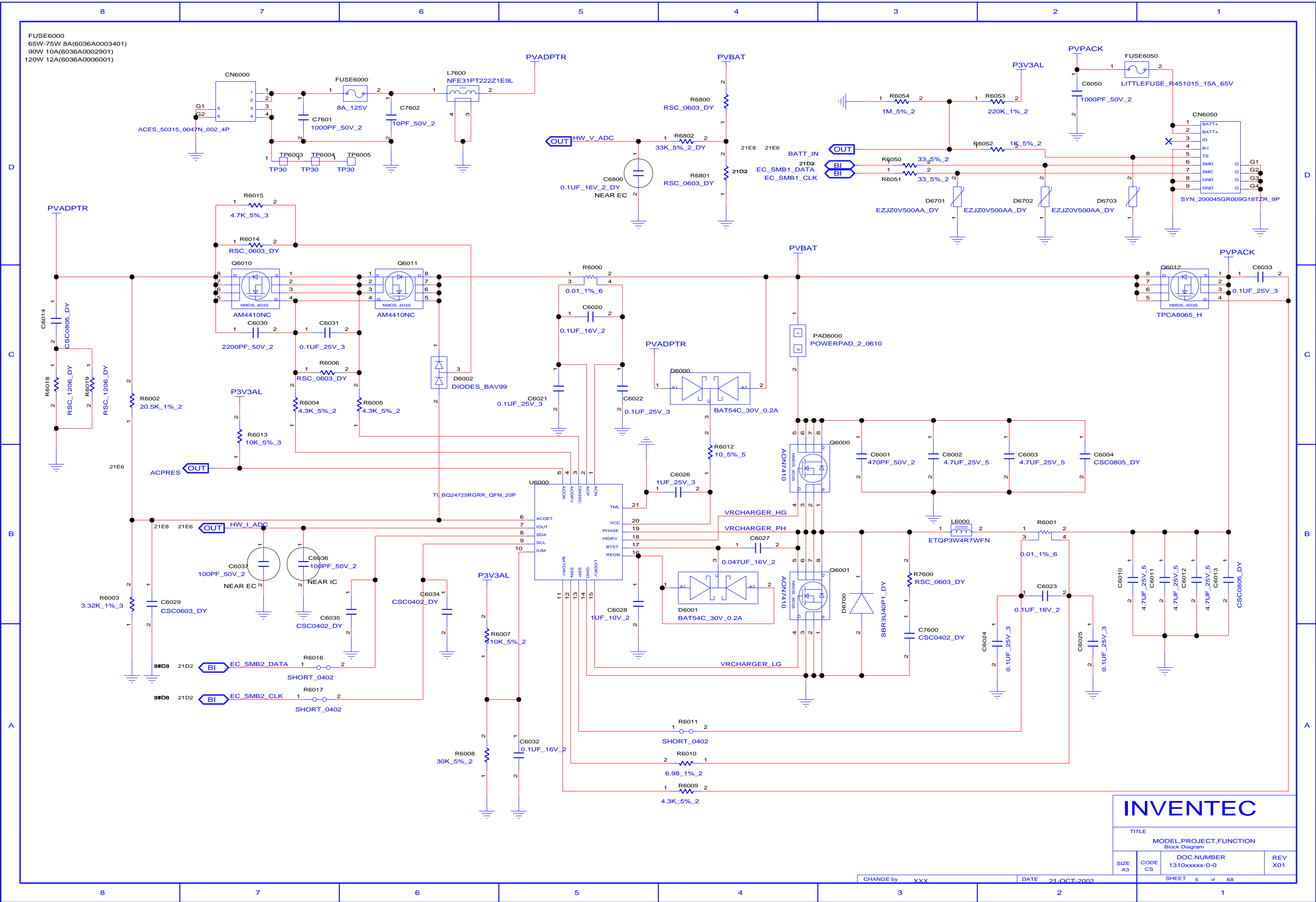
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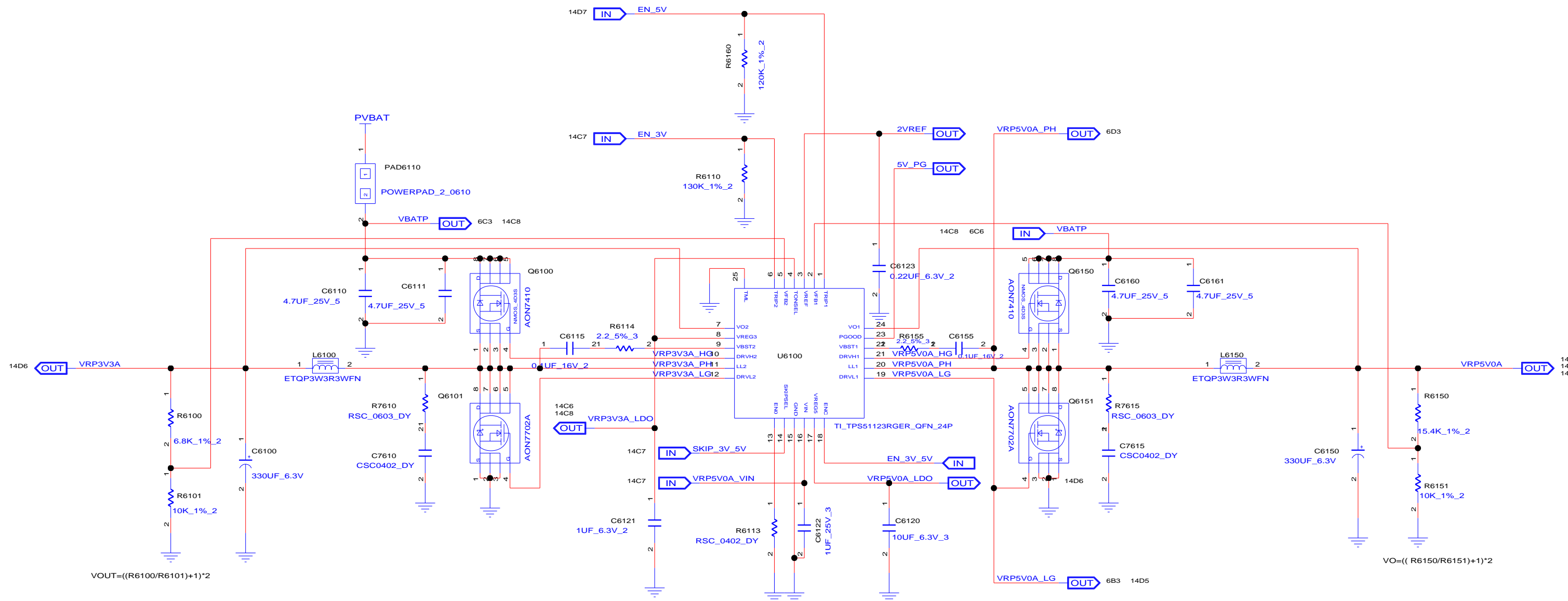
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Block Diagram		
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A2	CS	1310xxxxx-0-0



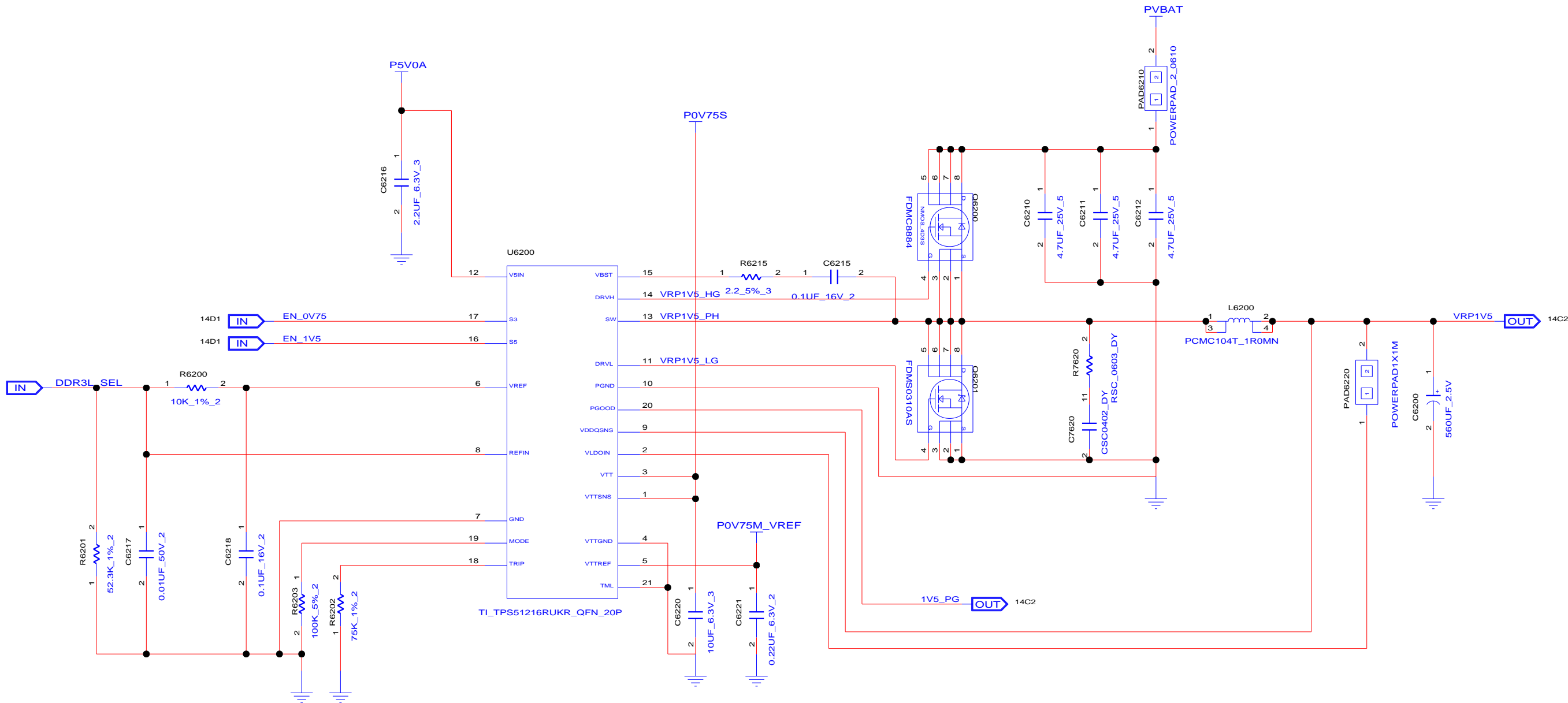




INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01


$$V_{OUT} = ((R_{6100}/R_{6101}) + 1) * 2$$

# INVENTEC



VOUT=REFIN=1.8\*(R6201/(R6200+R6201))  
MODE=100KOHM:TRACKING DISCHARGE

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

INVENTEC

TITLE

MODEL,PROJECT,FUNCTION  
Block Diagram

SIZE  
A3

CODE  
CS

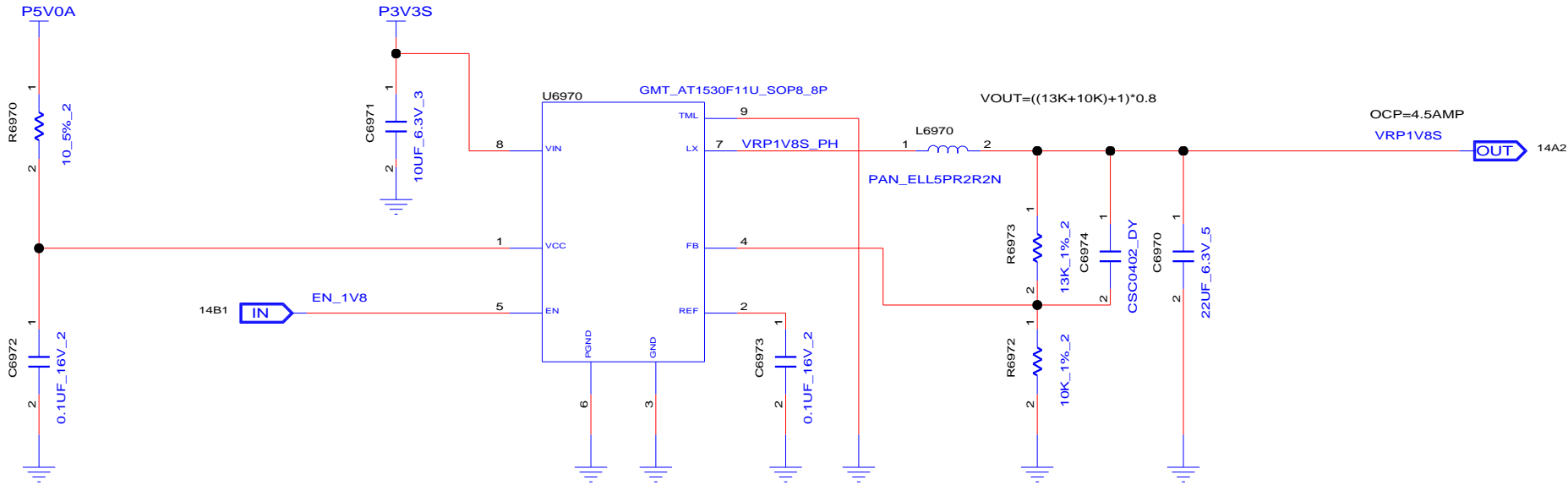
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X01

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INVENTEC

TITLE  
MODEL,PROJECT,FUNCTION  
Block Diagram

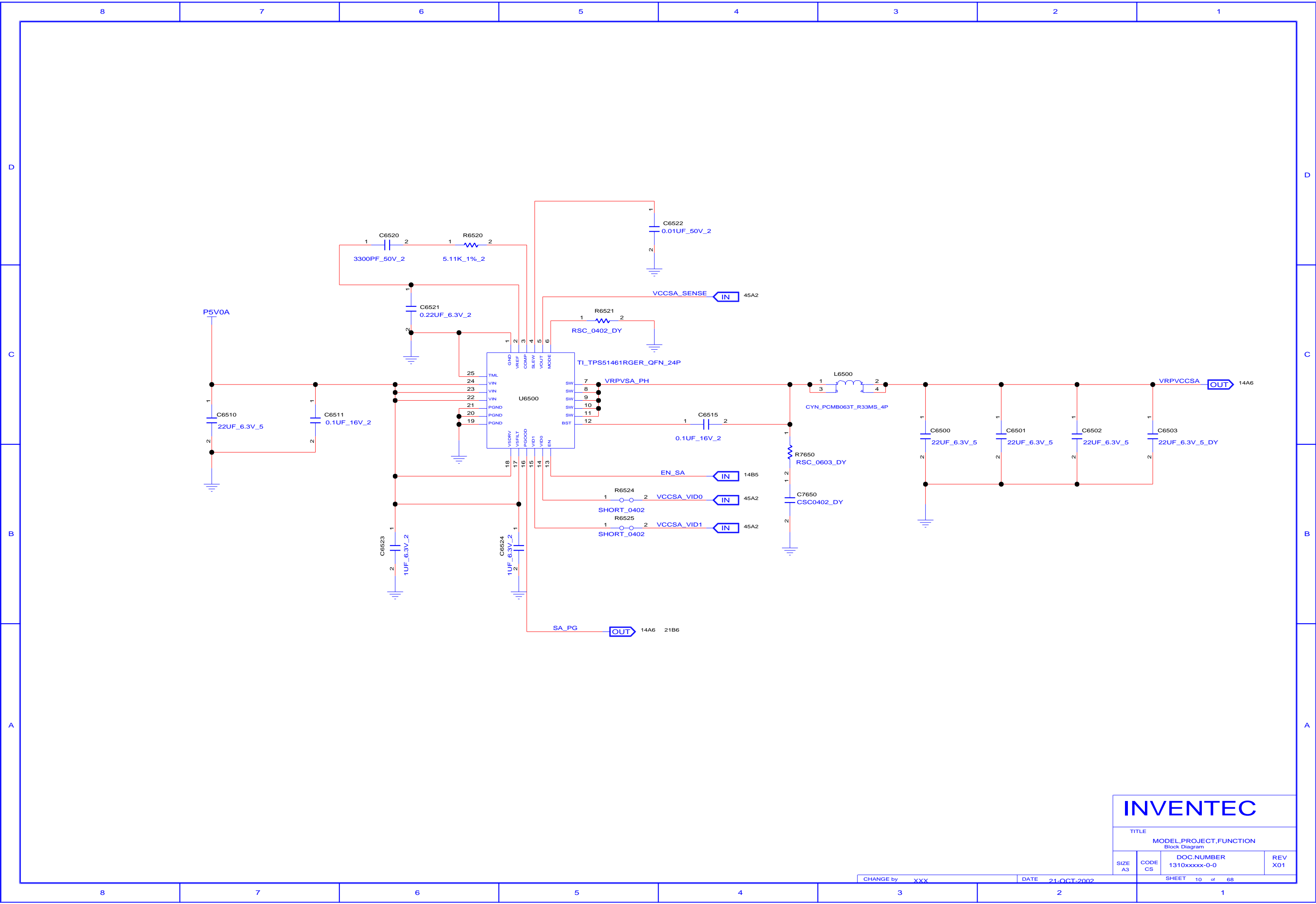
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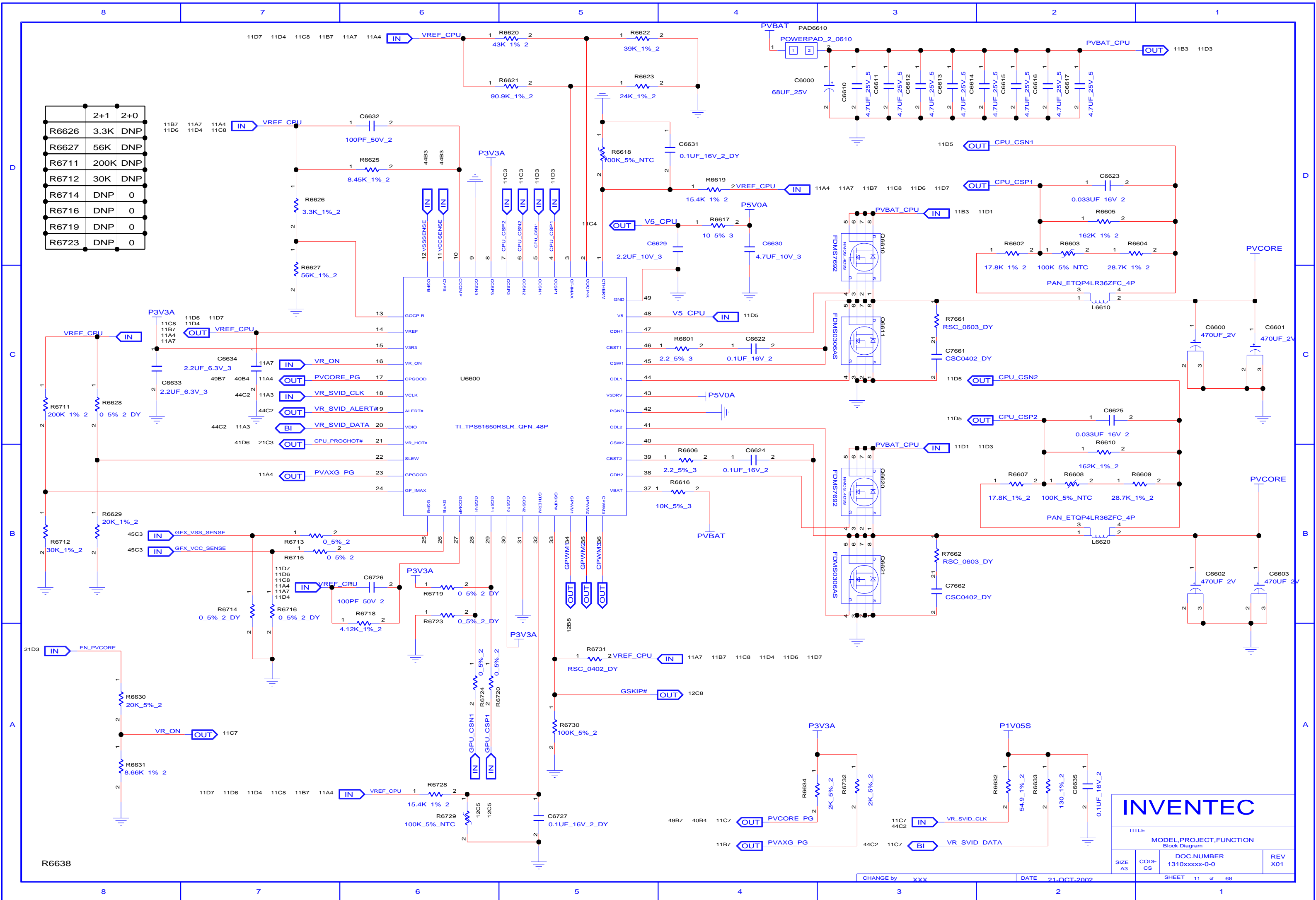
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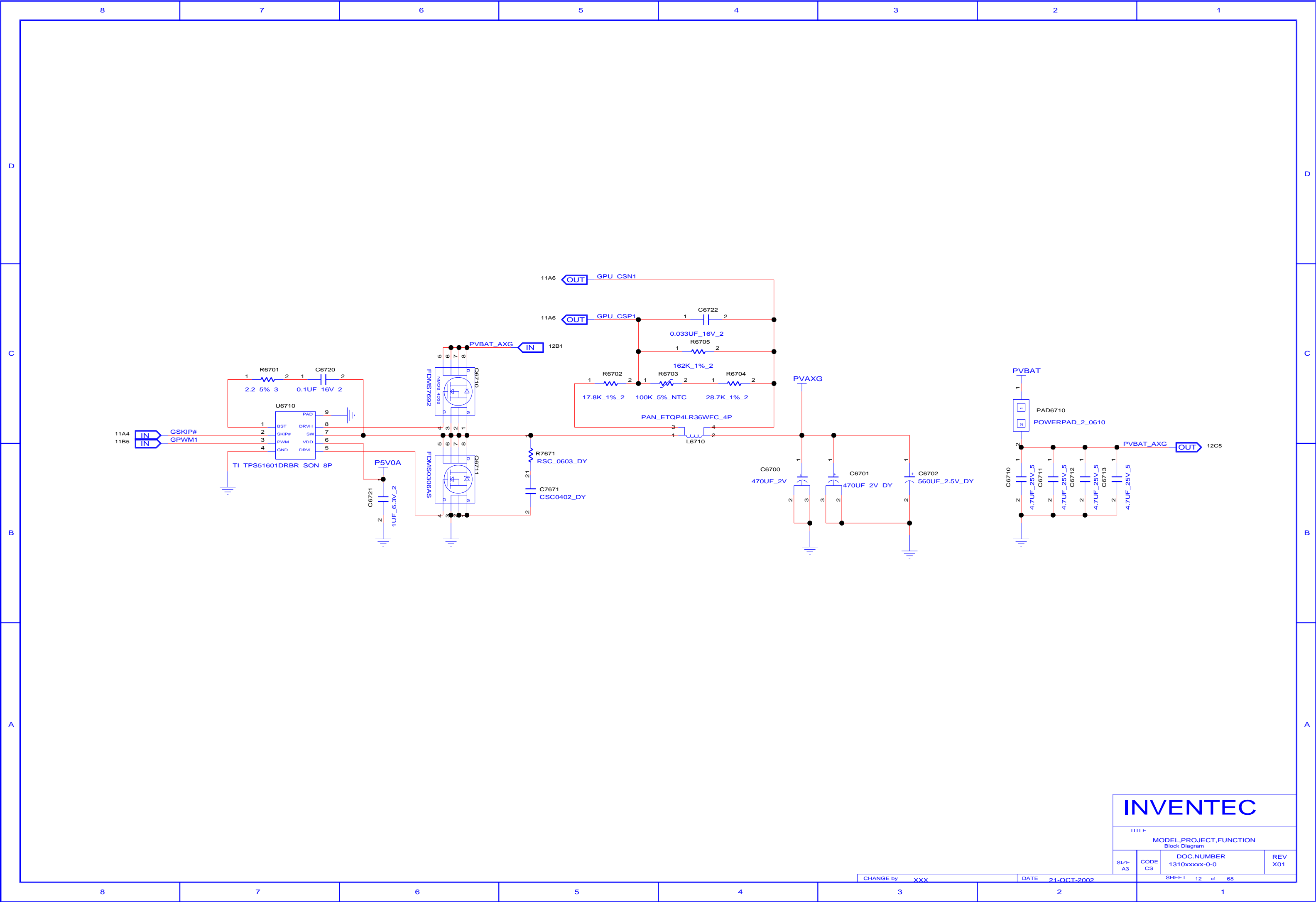
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INVENTEC

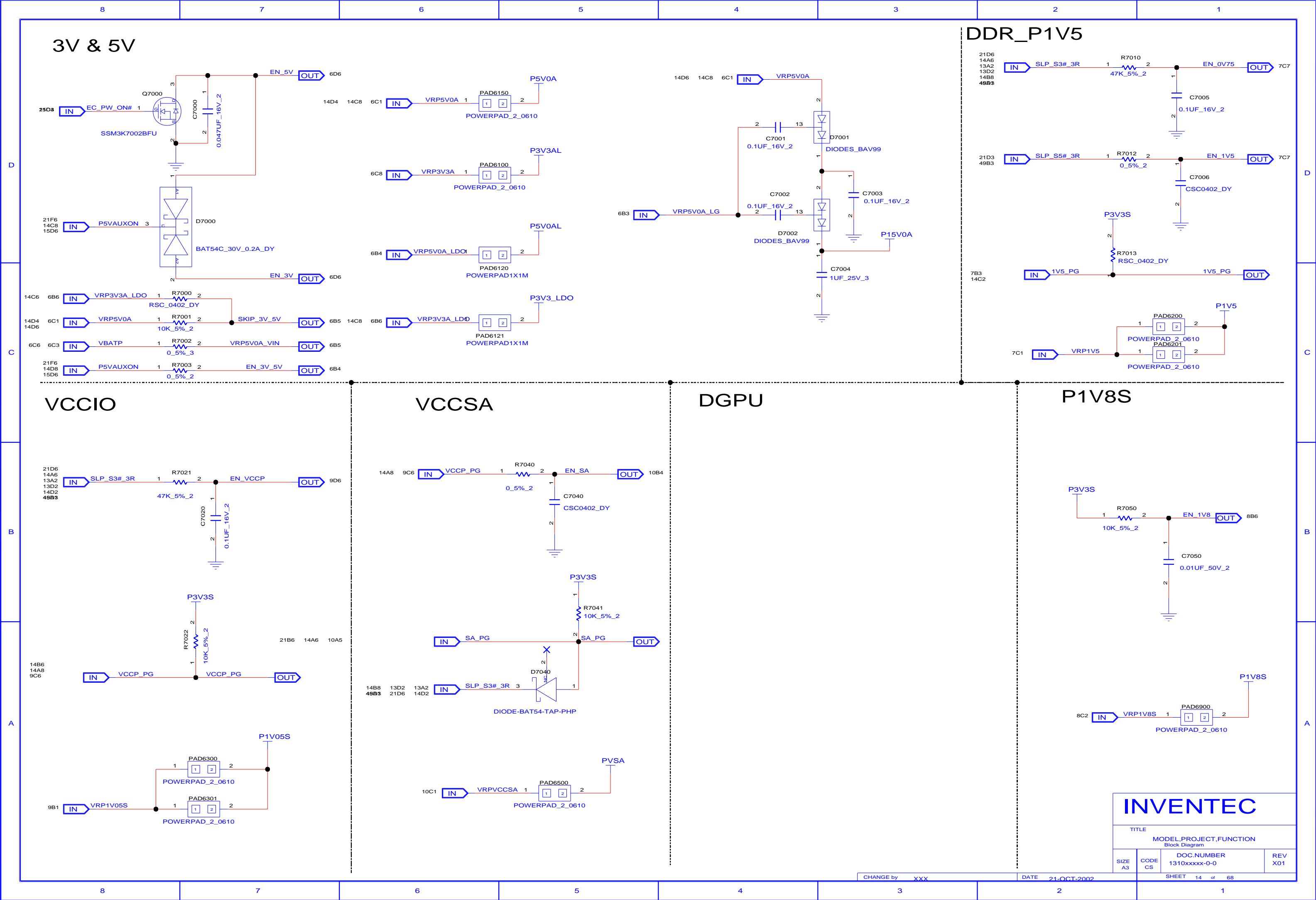
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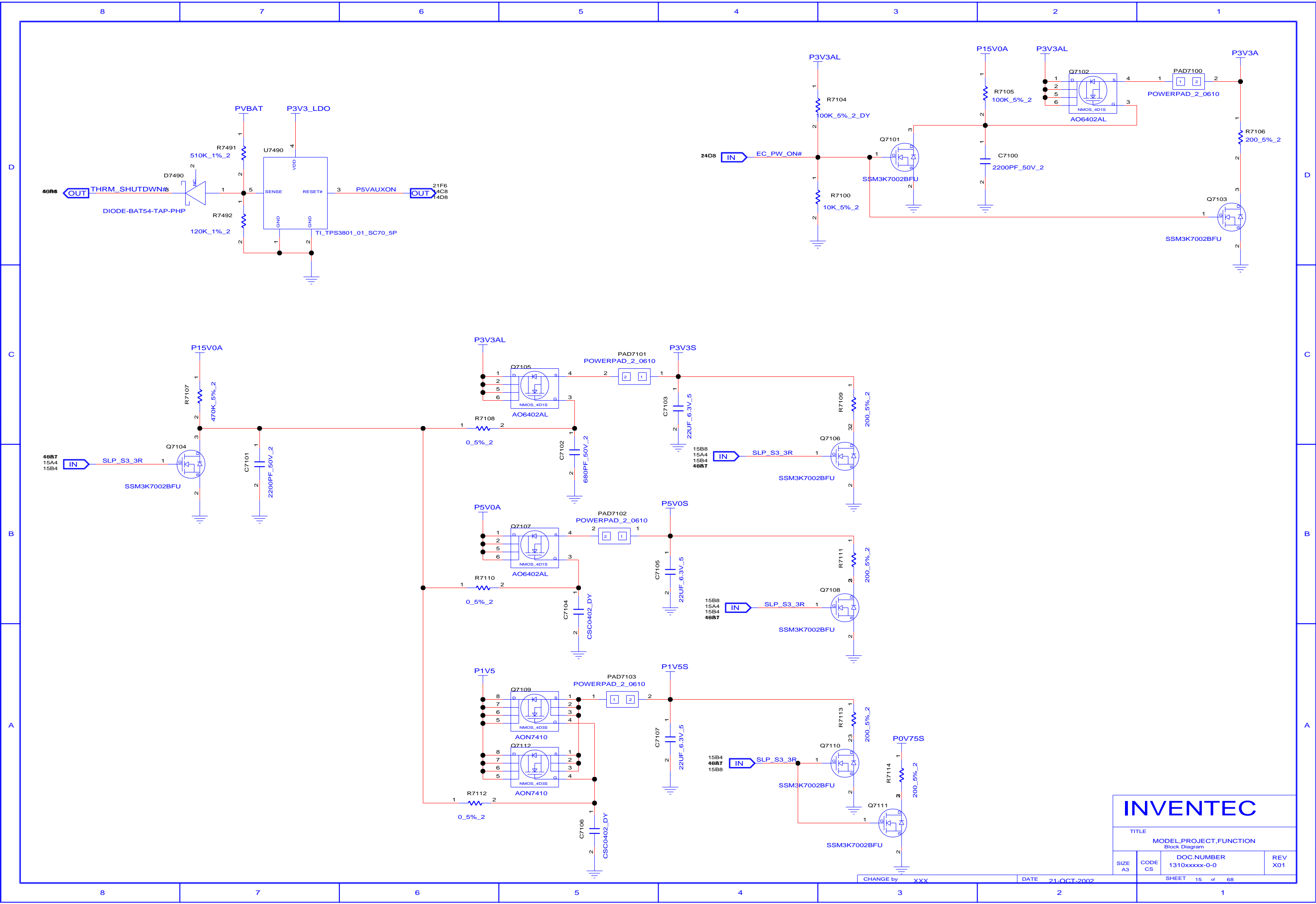
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INVENTEC

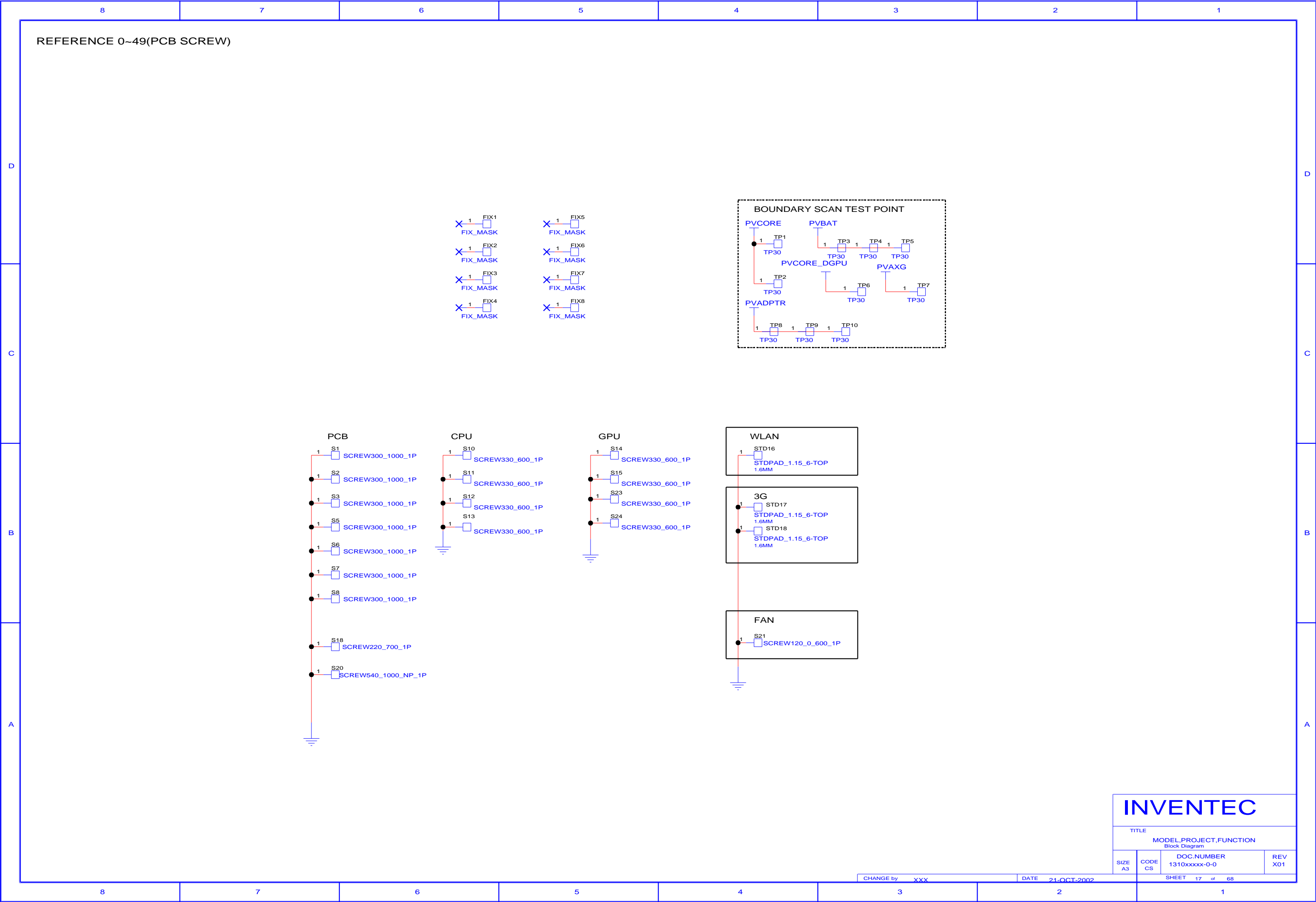
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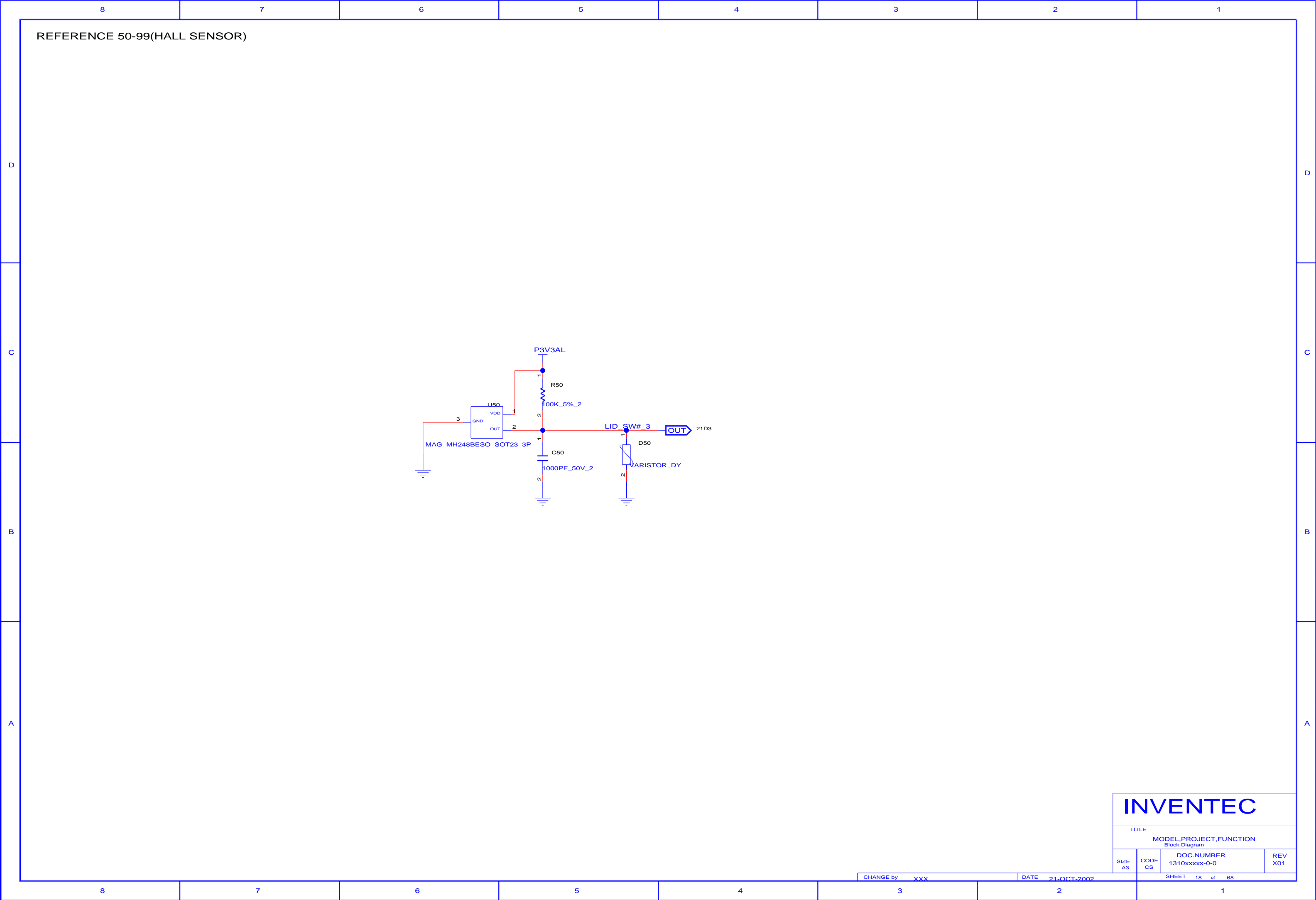
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INVENTEC

TITLE

MODEL,PROJECT,FUNCTION

Block Diagram

SIZE

A3

CODE

CS

DOC.NUMBER

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X01

CHANGE by

XXX

DATE

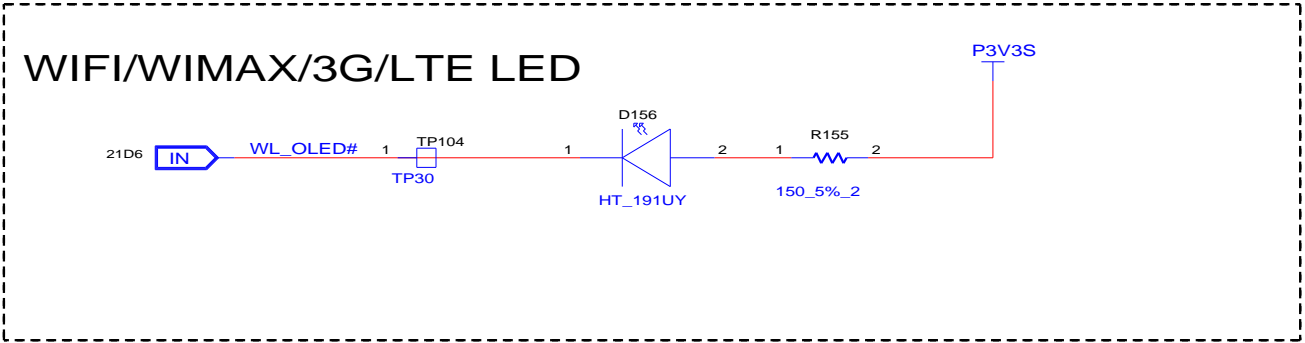
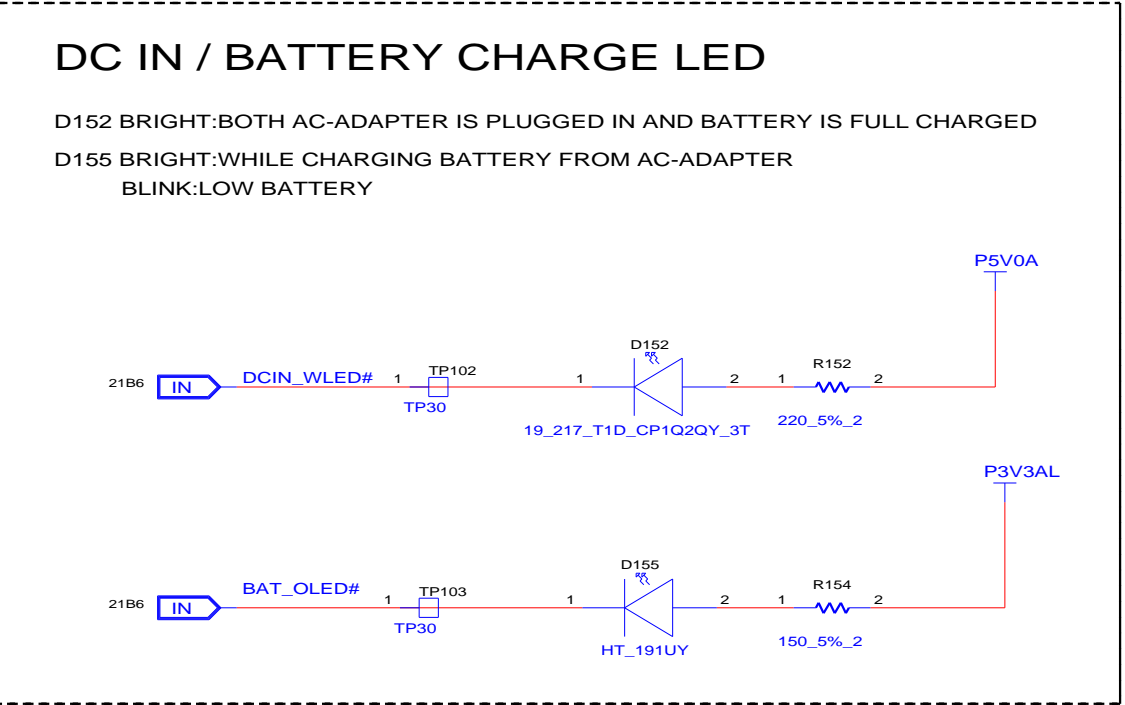
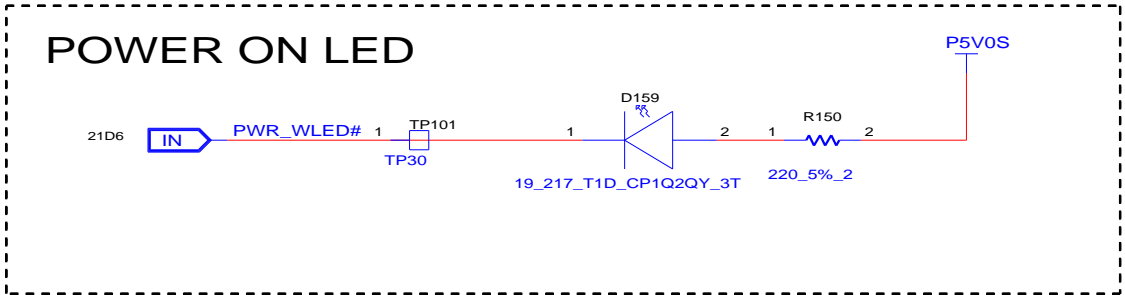
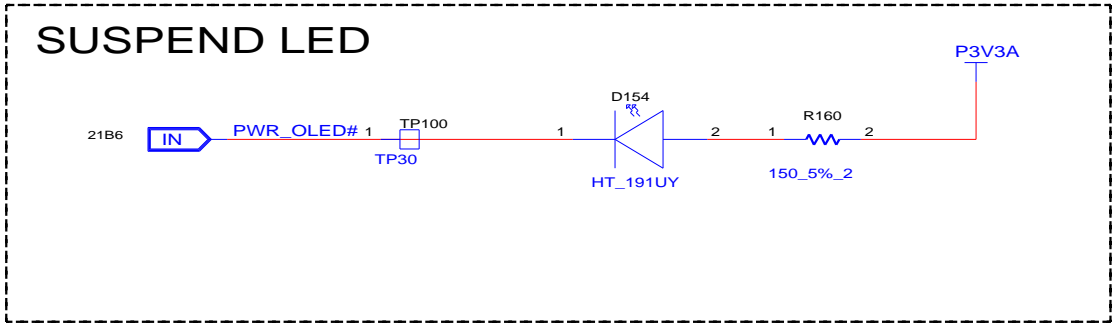
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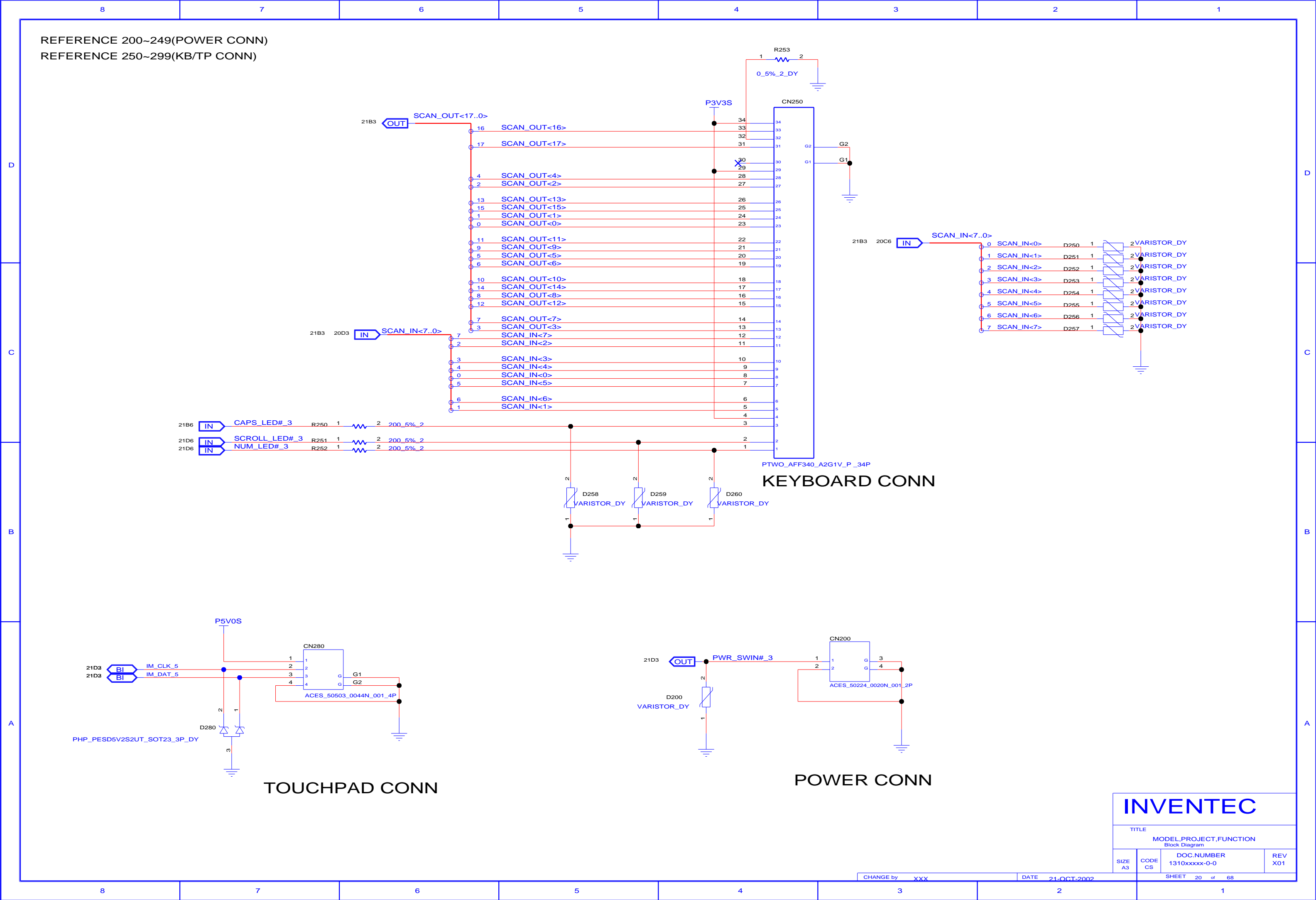
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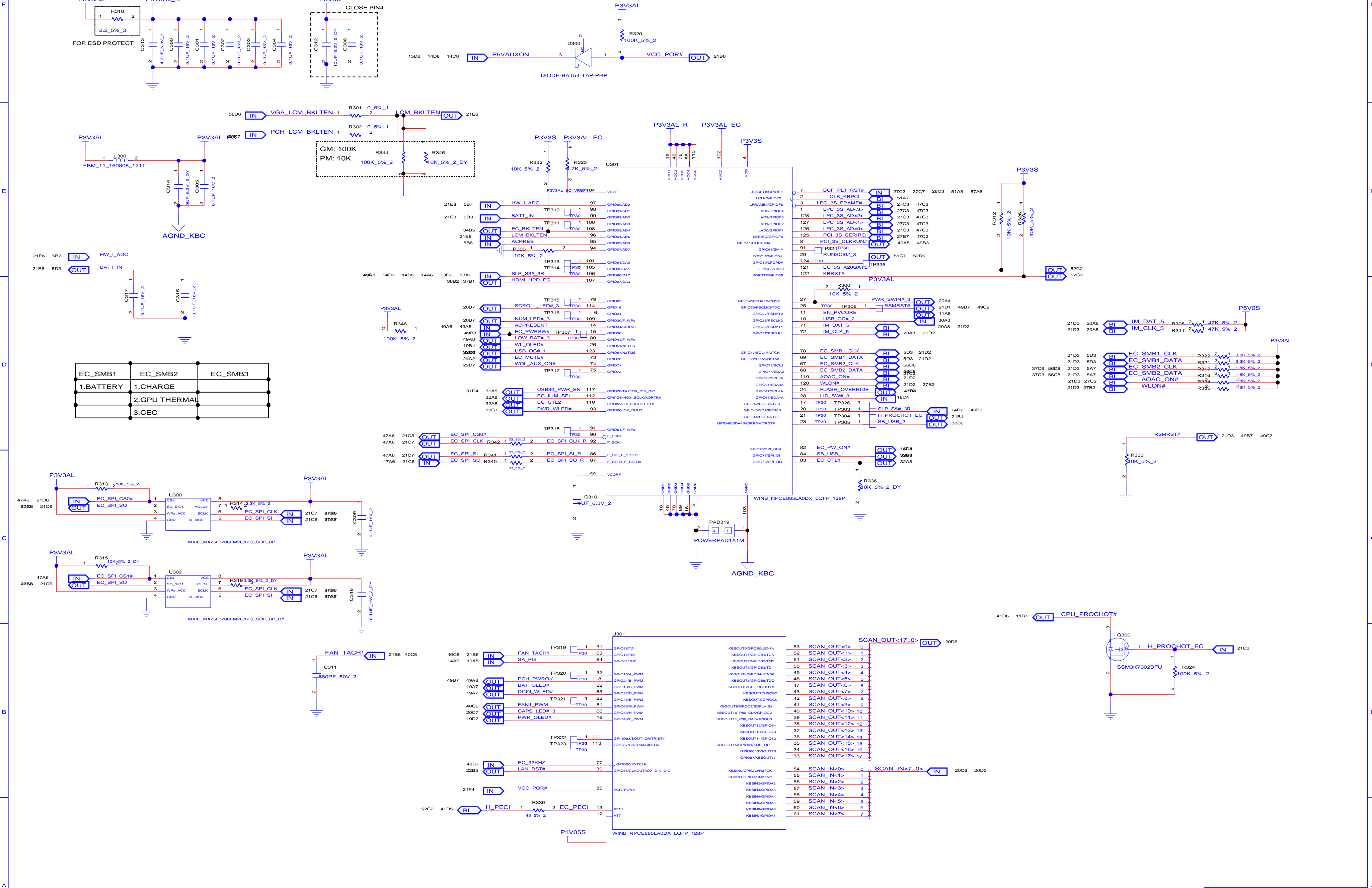
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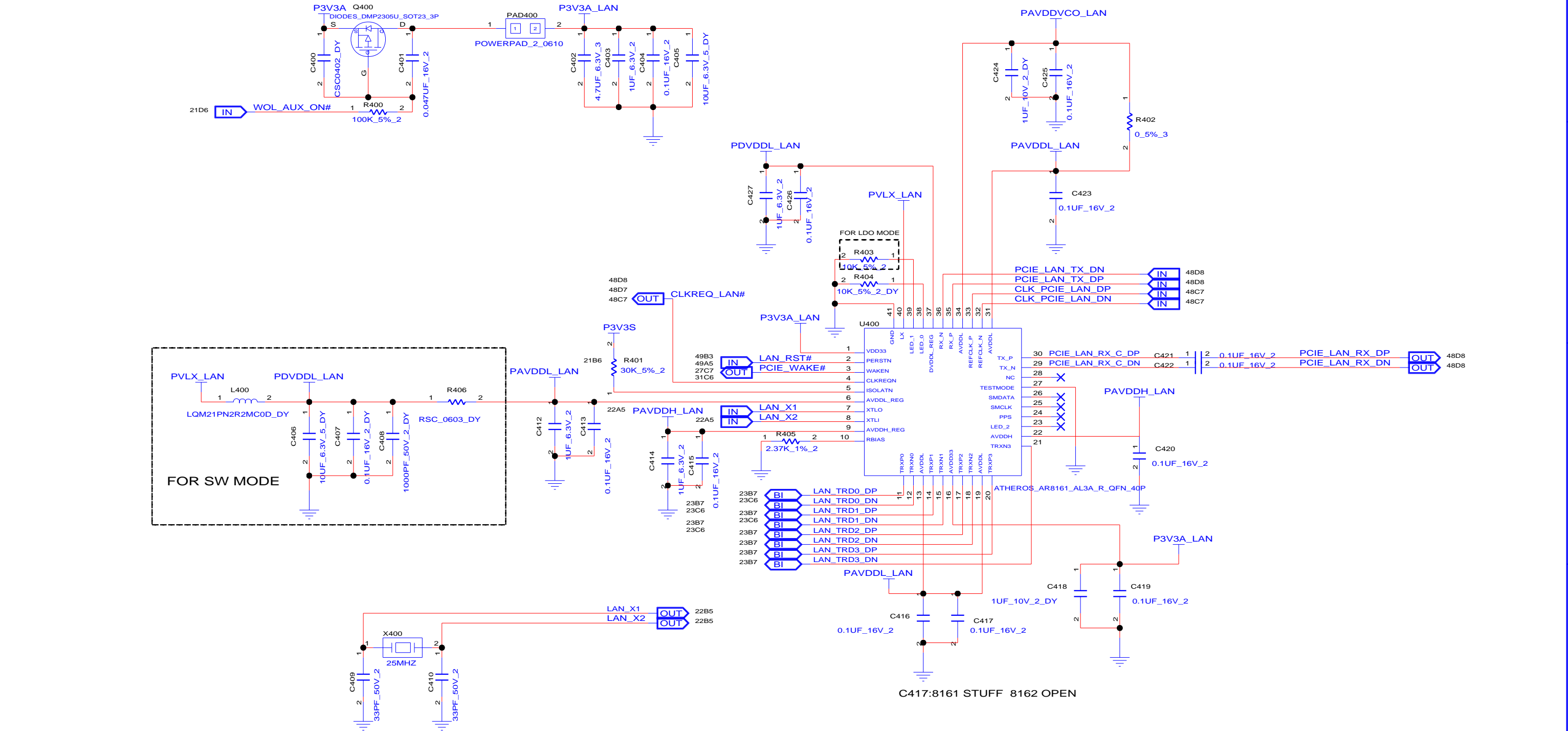
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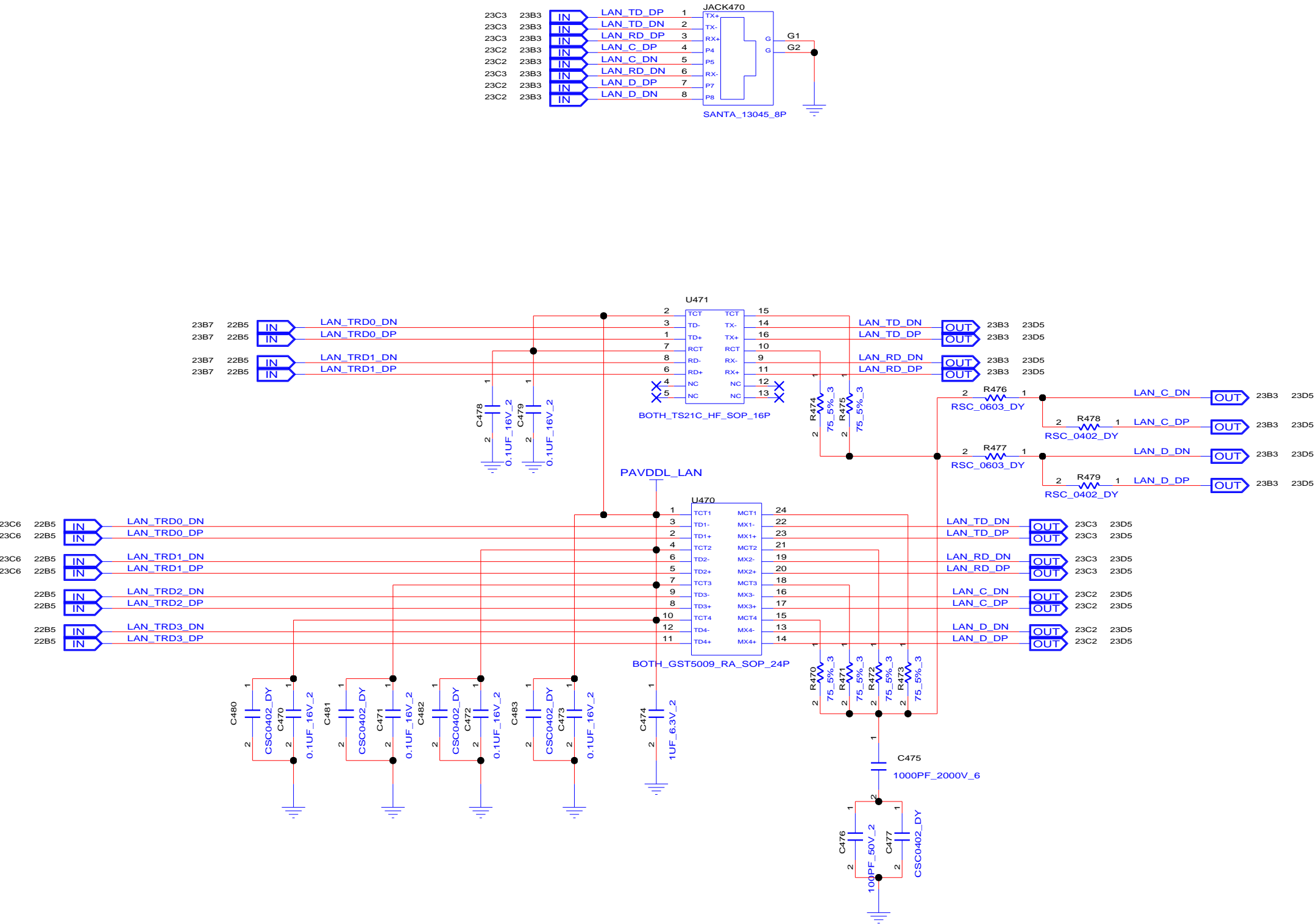


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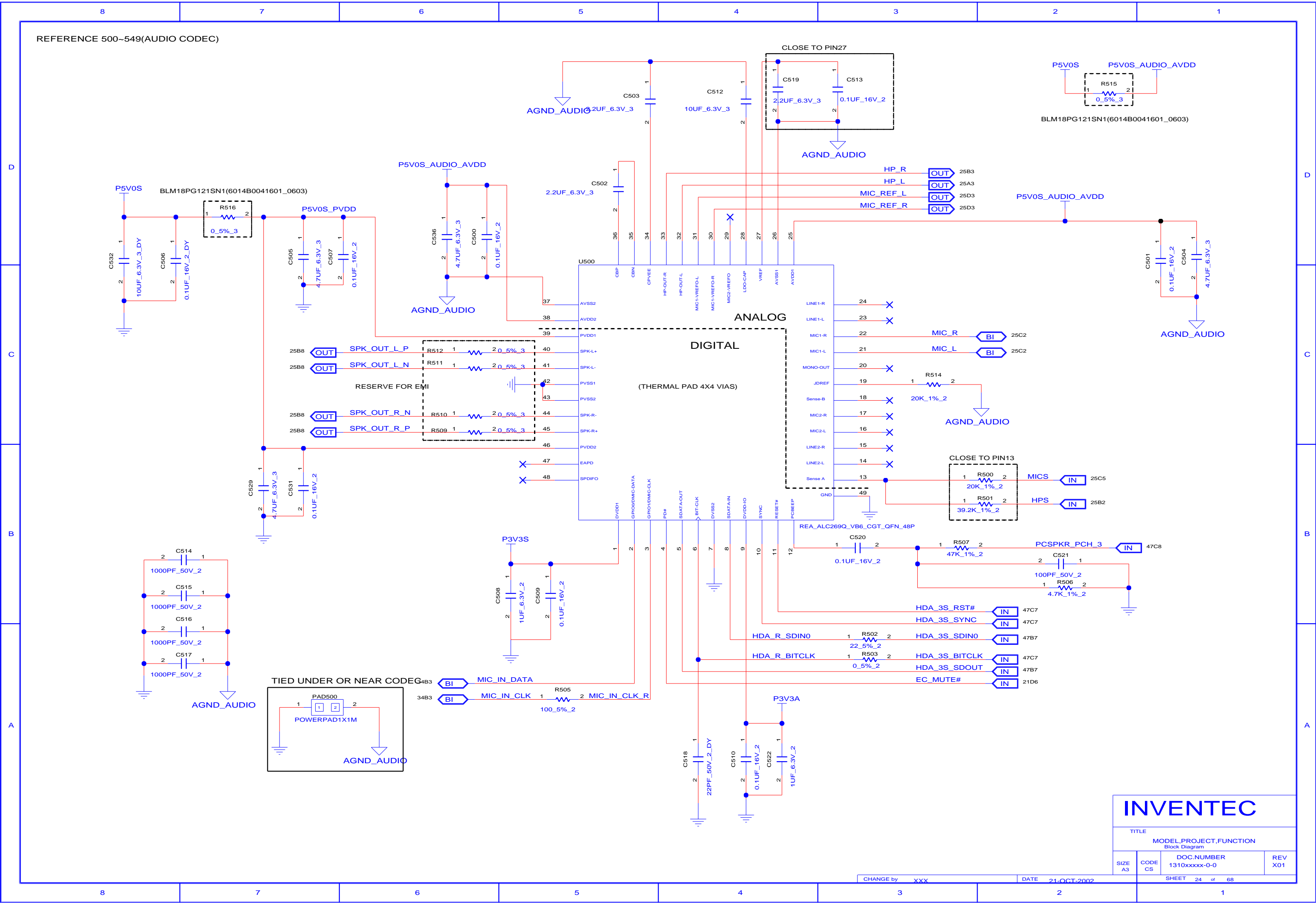


AS	CS	
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REFERENCE 400~499(LAN)



INVENTEC			
TITLE			
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A3	CS	1310xxxx-0-0	X01

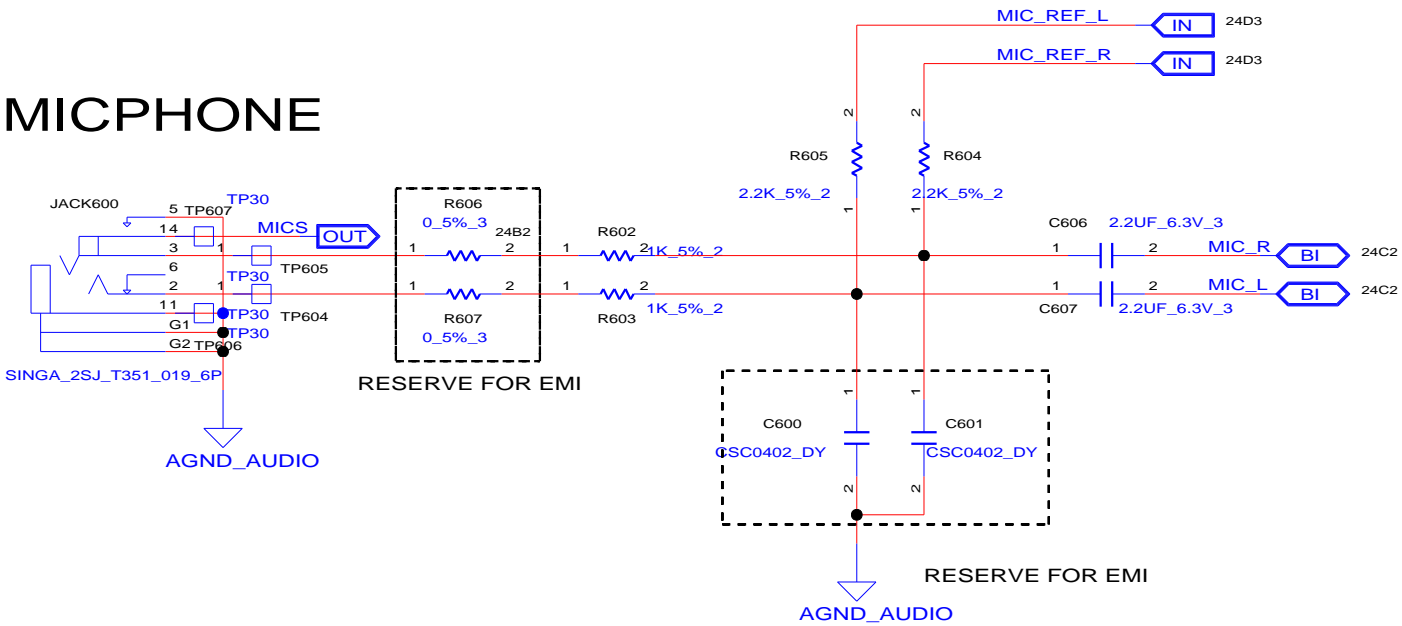


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MODEL,PROJECT,FUNCTION Block Diagram			
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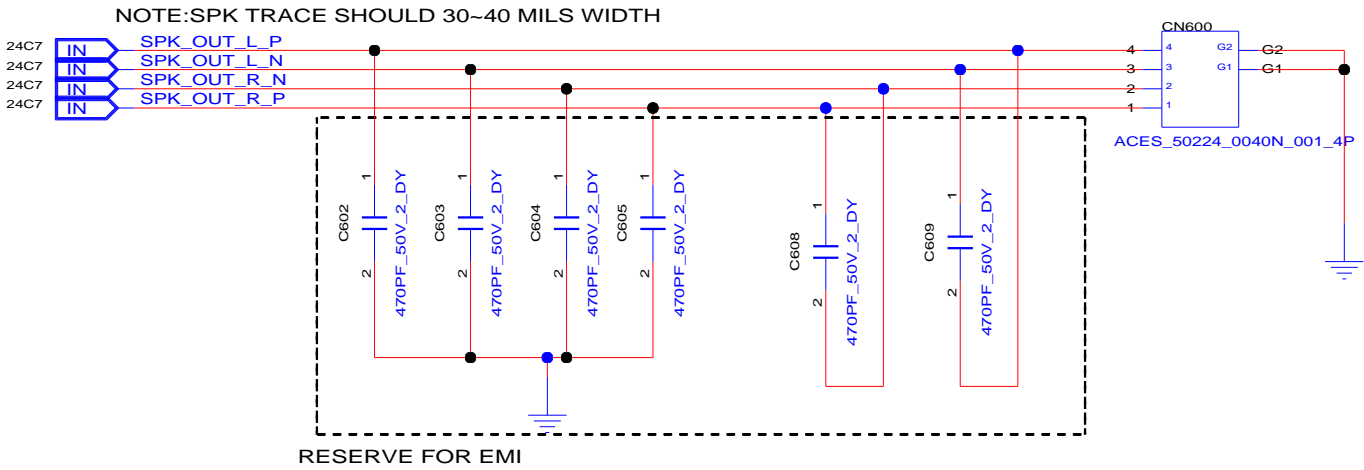


# AUDIO JACKS

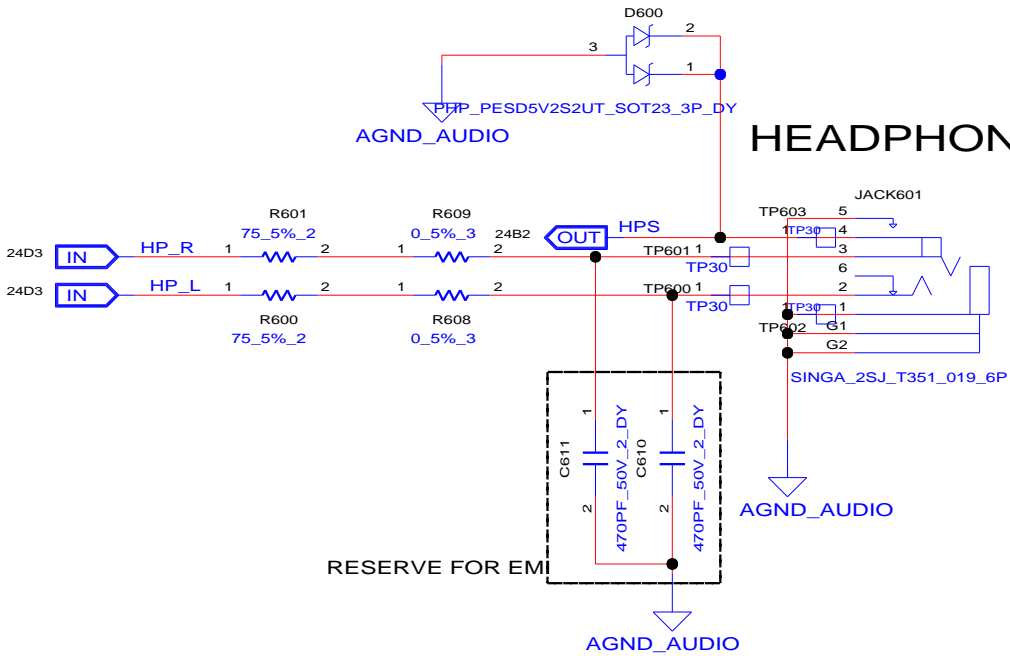
## MICPHONE



## INTERNAL SPEAKERS



## HEADPHONE



INVENTEC

TITLE

MODEL,PROJECT,FUNCTION

Block Diagram

SIZE A3 CODE CS

DOC.NUMBER 1310xxxx-0-0

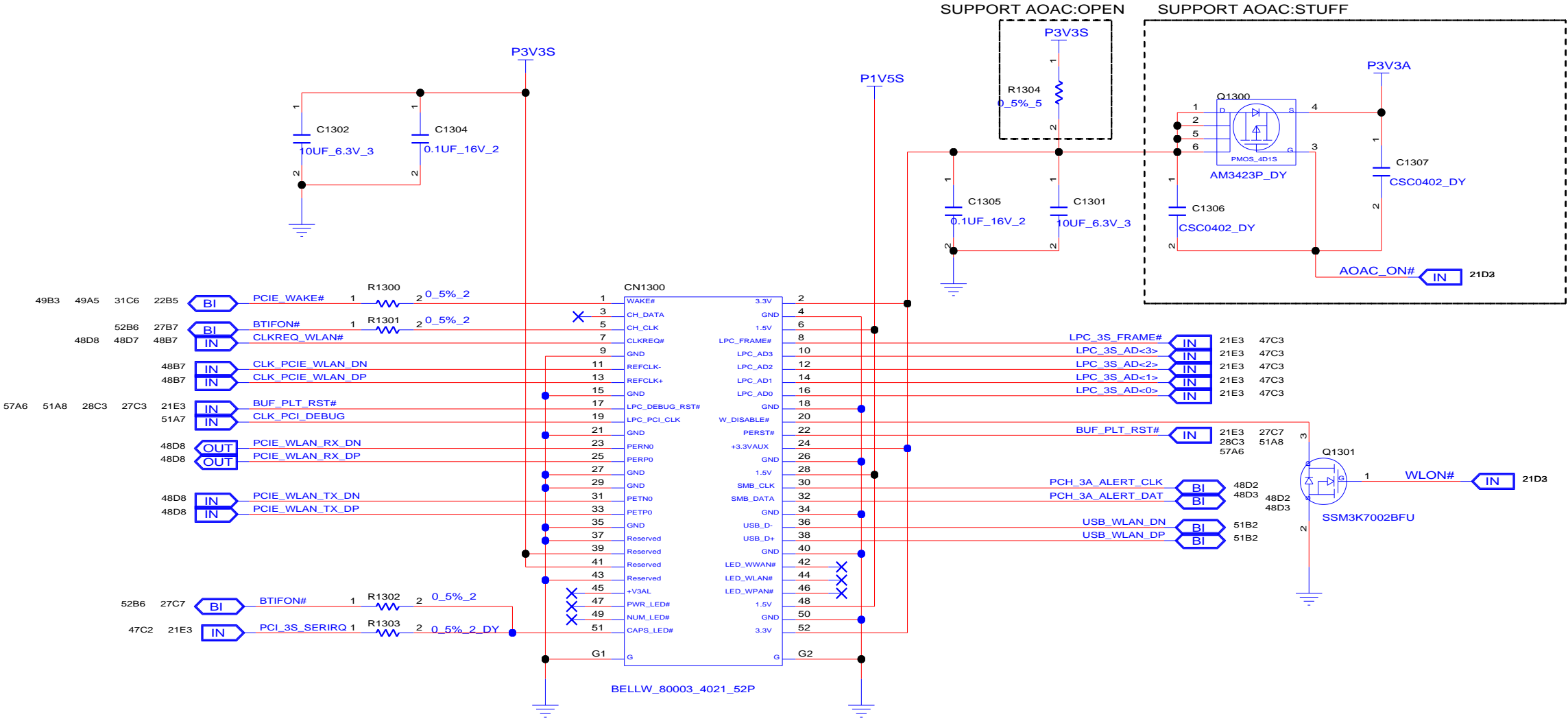
REV X01

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## A

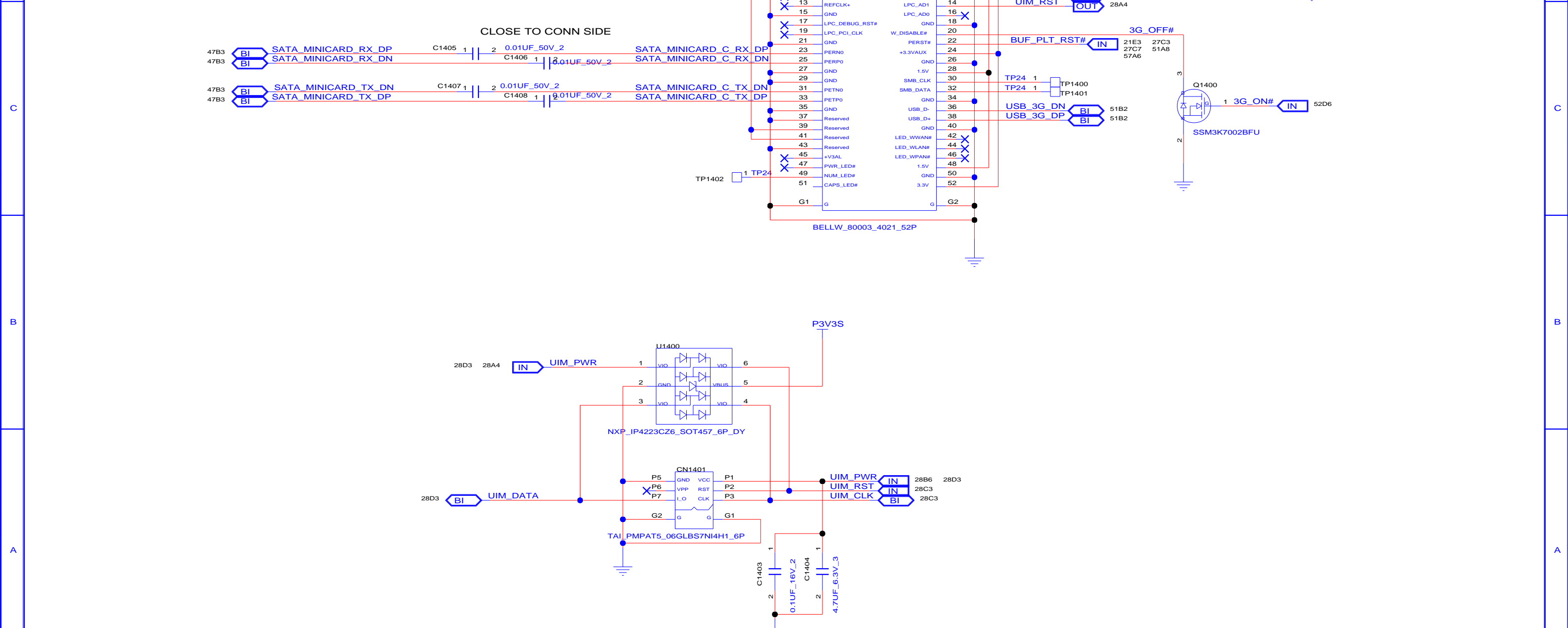
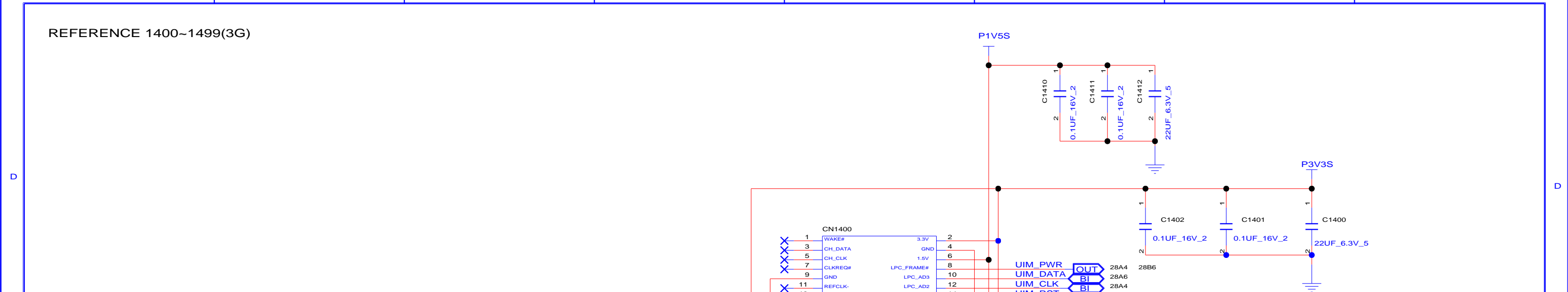




MINI CARD 1(WLAN)

INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

8	7	6	5	4	3	2	1
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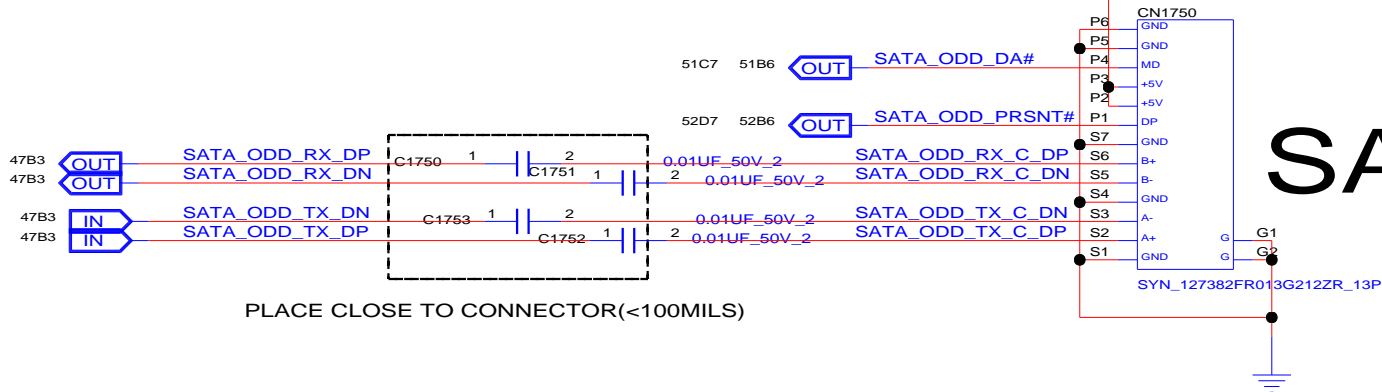
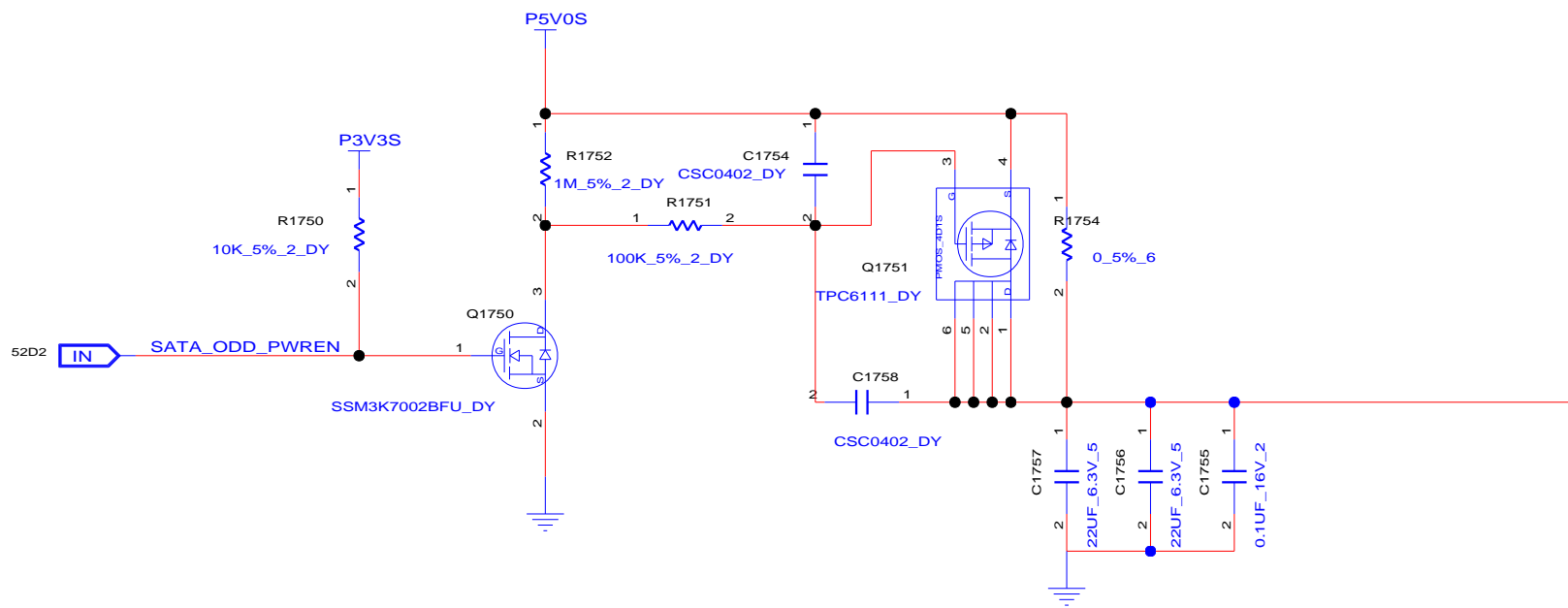
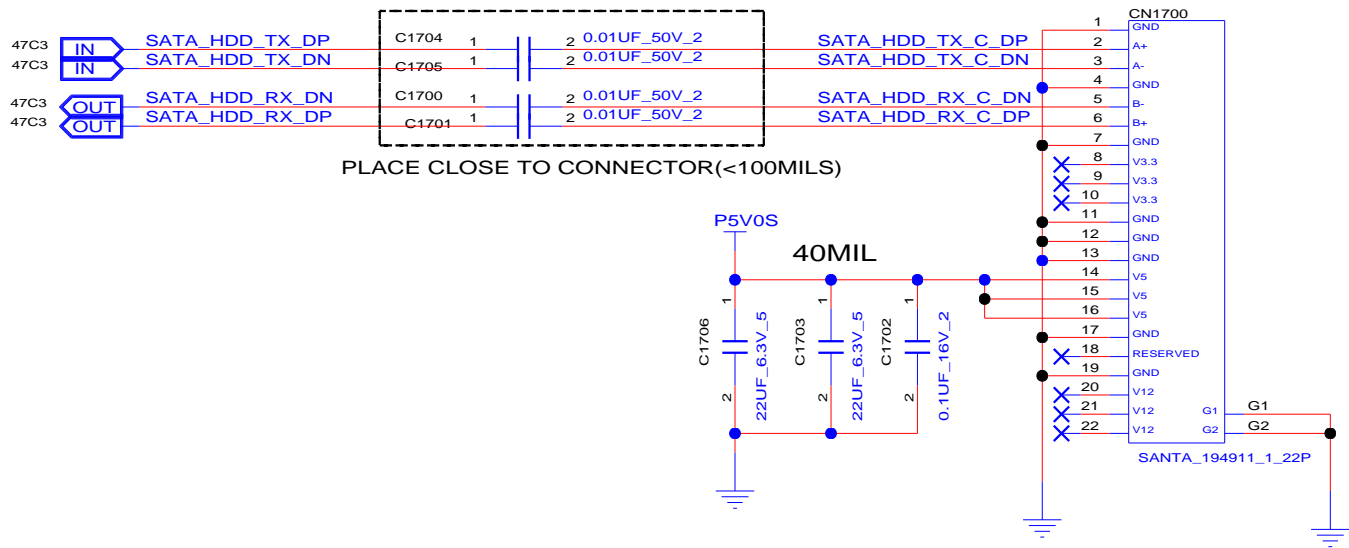


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REFERENCE 1700~1749(HDD)  
REFERENCE 1750~1799(ODD)

# SATA HDD



# SATA ODD

INVENTEC

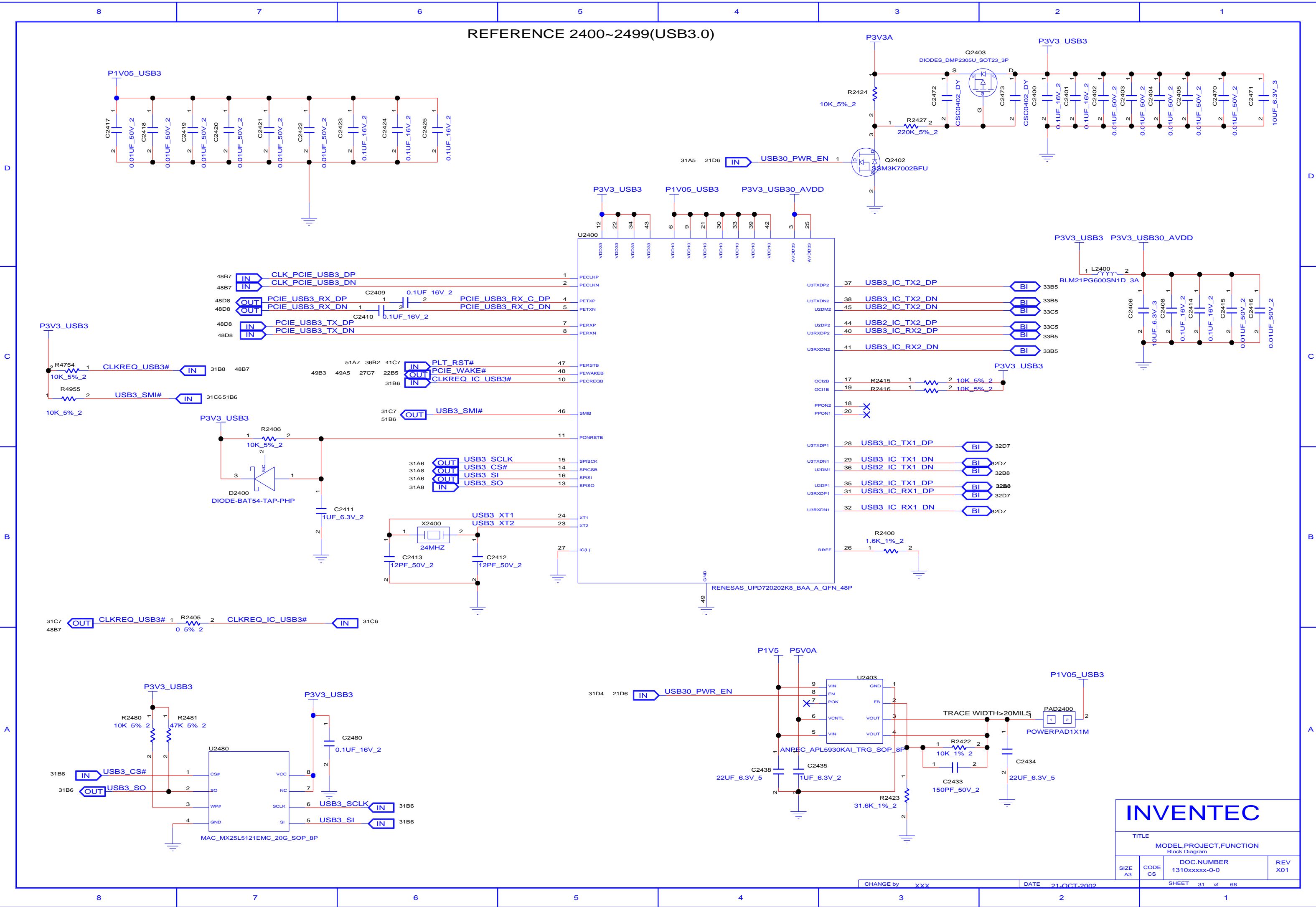
TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01

CHANGE by XXX DATE 21-OCT-2002

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REFERENCE 2400~2499(USB3.0)



INVENTEC

TITLE

MODEL,PROJECT,FUNCTION

Block Diagram

SIZE A3

CODE CS

DOC.NUMBER

1310xxxx-0-0

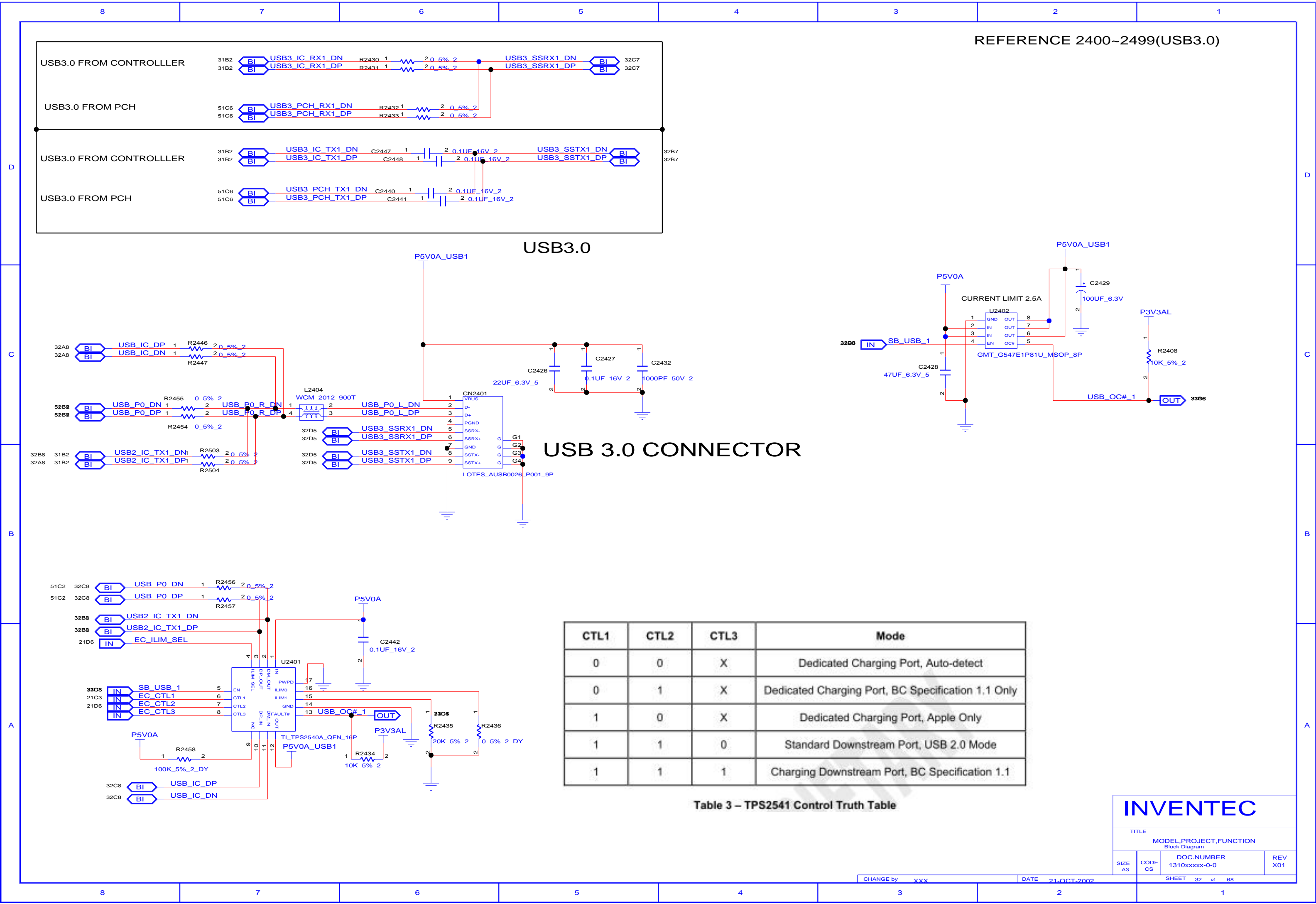
REV

X01

CHANGE by XXX

DATE 21-OCT-2002

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REFERENCE 2400~2499(USB3.0)

USB3.0

USB 3.0 CONNECTOR

CTL1	CTL2	CTL3	Mode
0	0	X	Dedicated Charging Port, Auto-detect
0	1	X	Dedicated Charging Port, BC Specification 1.1 Only
1	0	X	Dedicated Charging Port, Apple Only
1	1	0	Standard Downstream Port, USB 2.0 Mode
1	1	1	Charging Downstream Port, BC Specification 1.1

Table 3 – TPS2541 Control Truth Table

INVENTEC

TITLE

MODEL,PROJECT,FUNCTION

Block Diagram

DOC.NUMBER

1310xxxxx-0-0

REV

X01

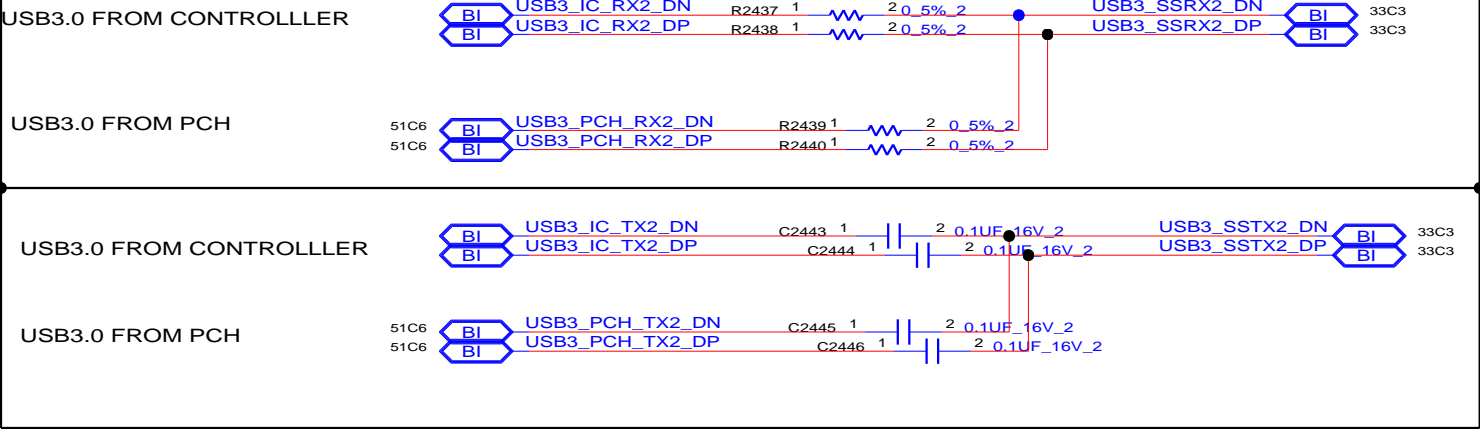
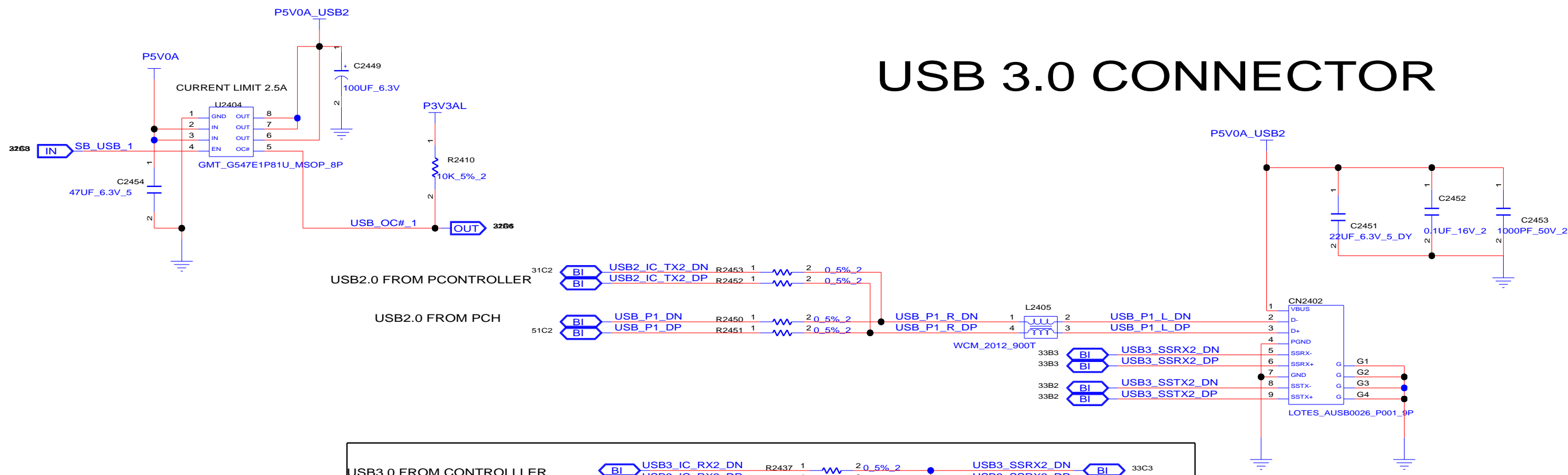
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REFERENCE 2400~2499(USB3.0)

# USB 3.0 CONNECTOR



USB3.0

INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

REFERENCE 3000~3049(LCM)

D

C

B

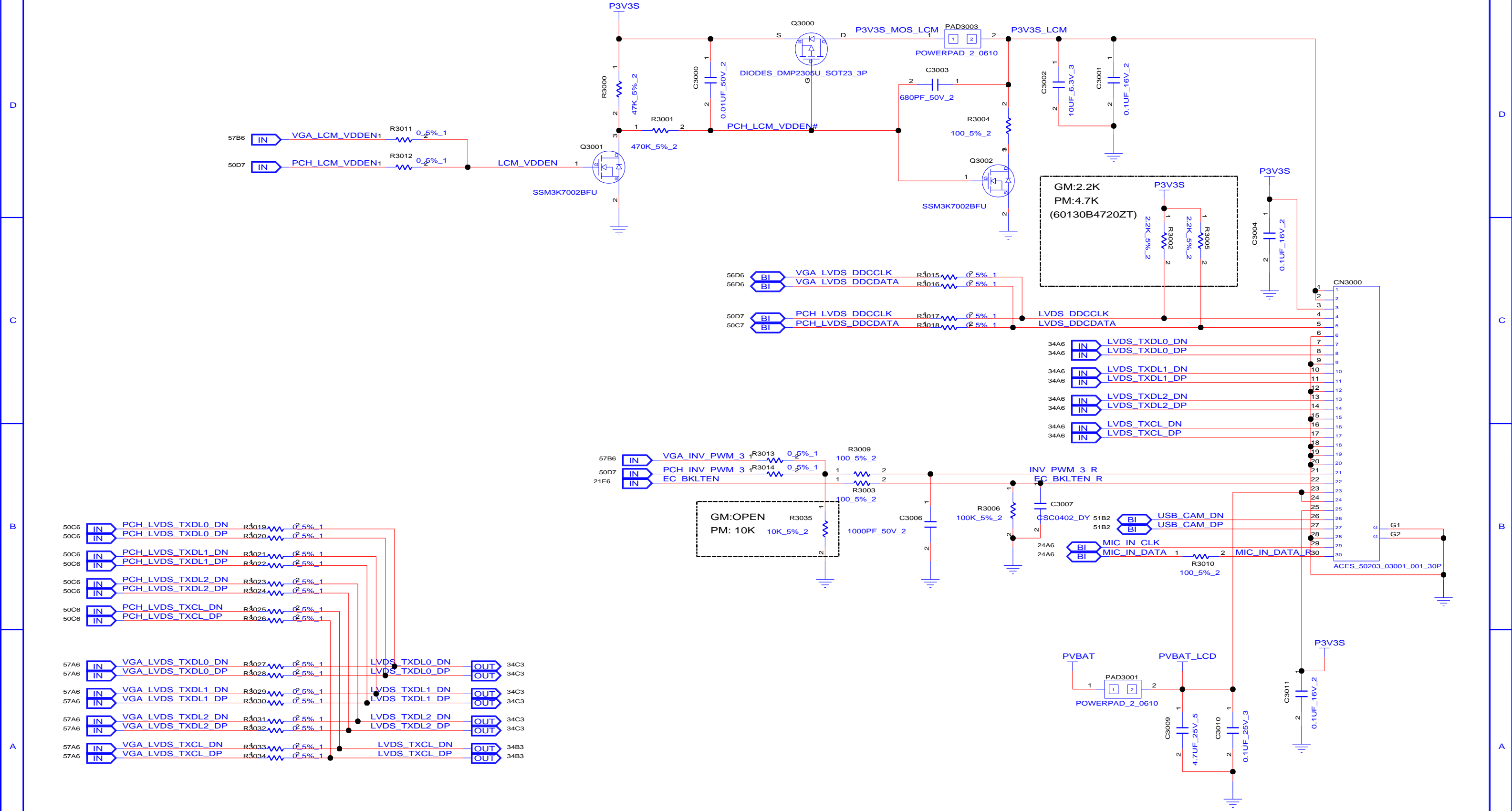
A

D

C

B

A

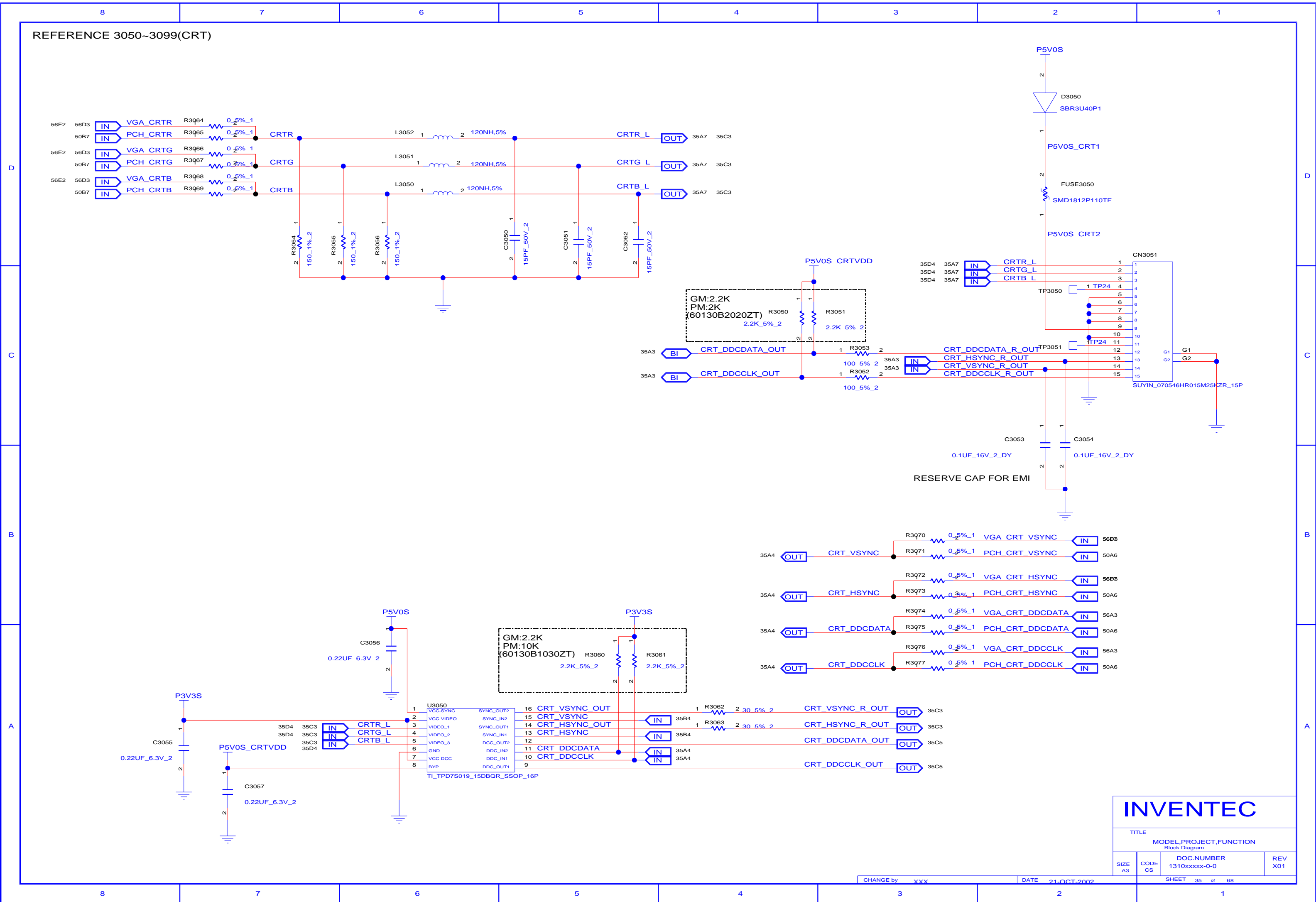


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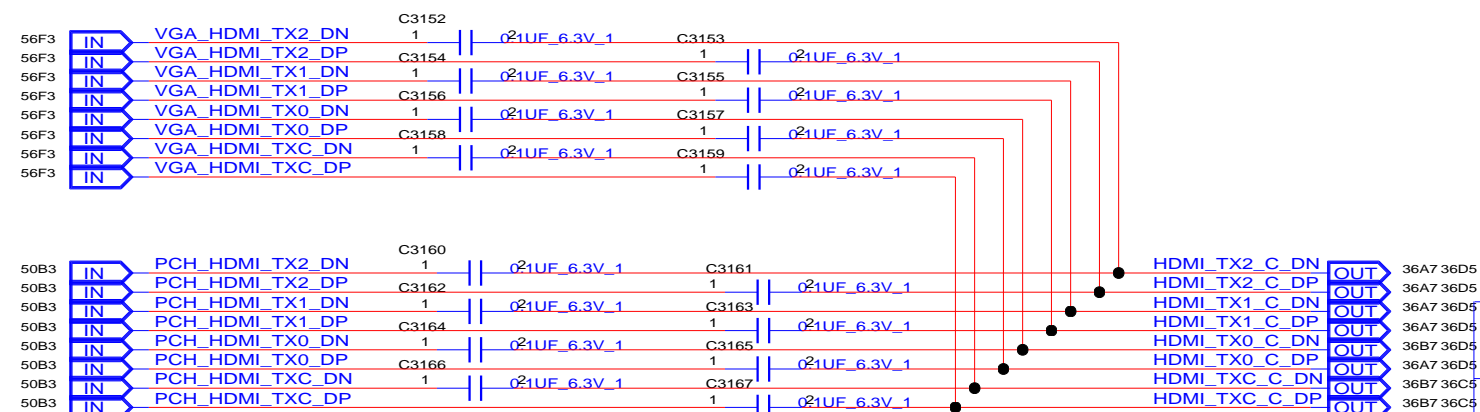
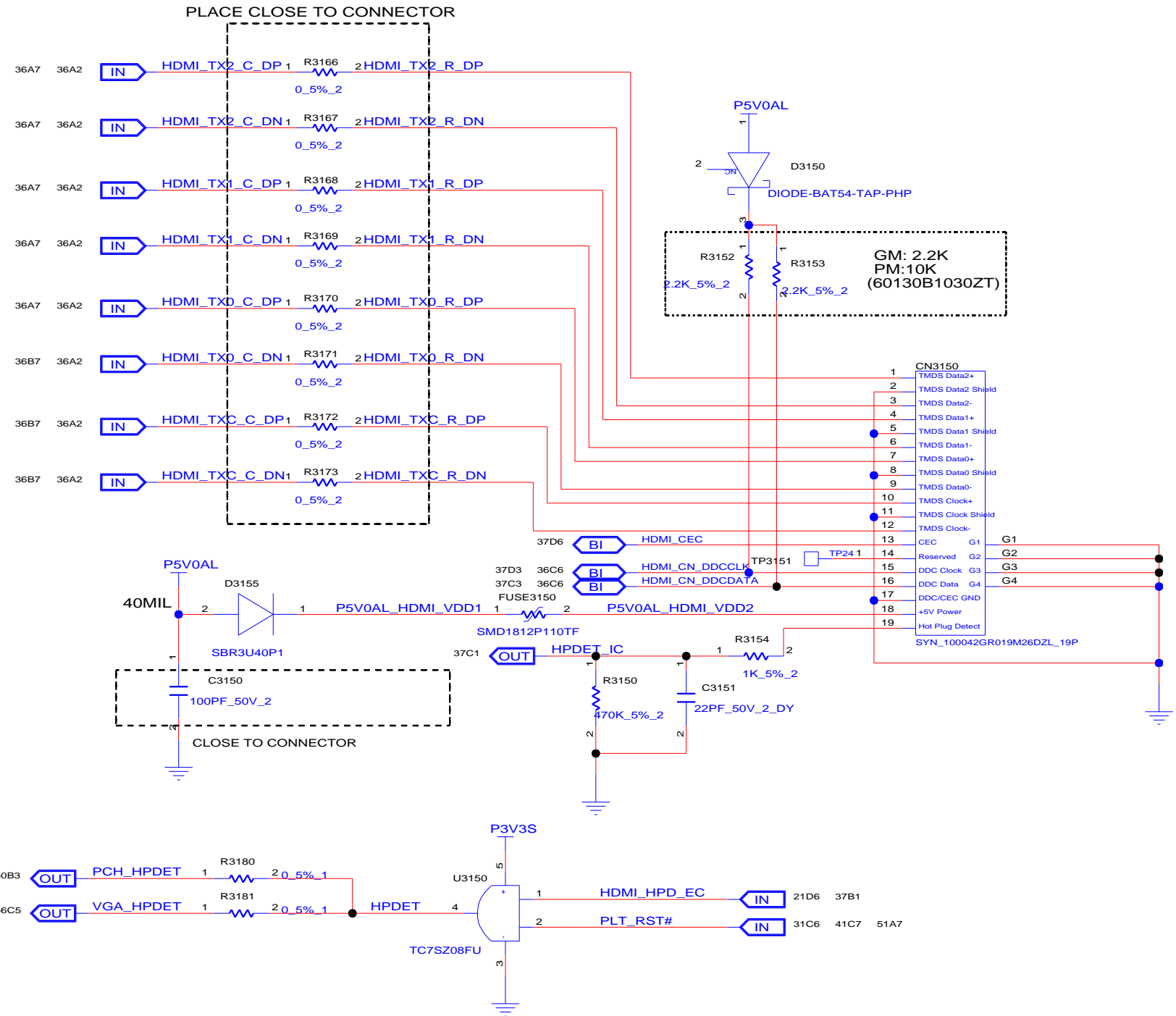
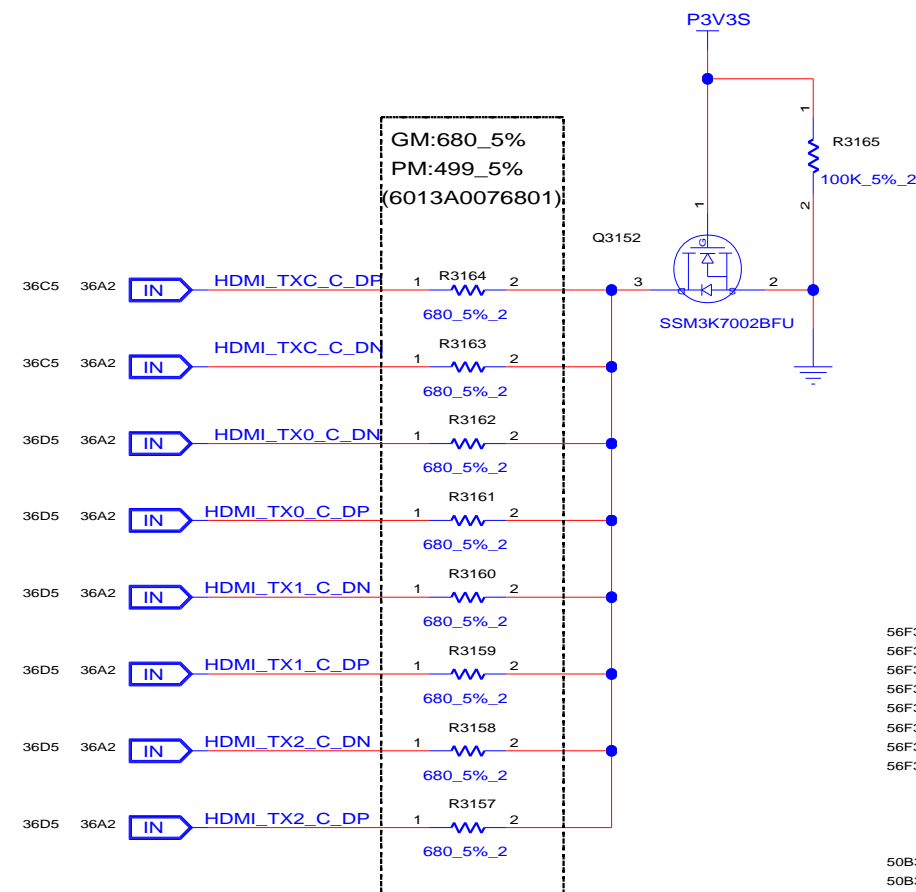
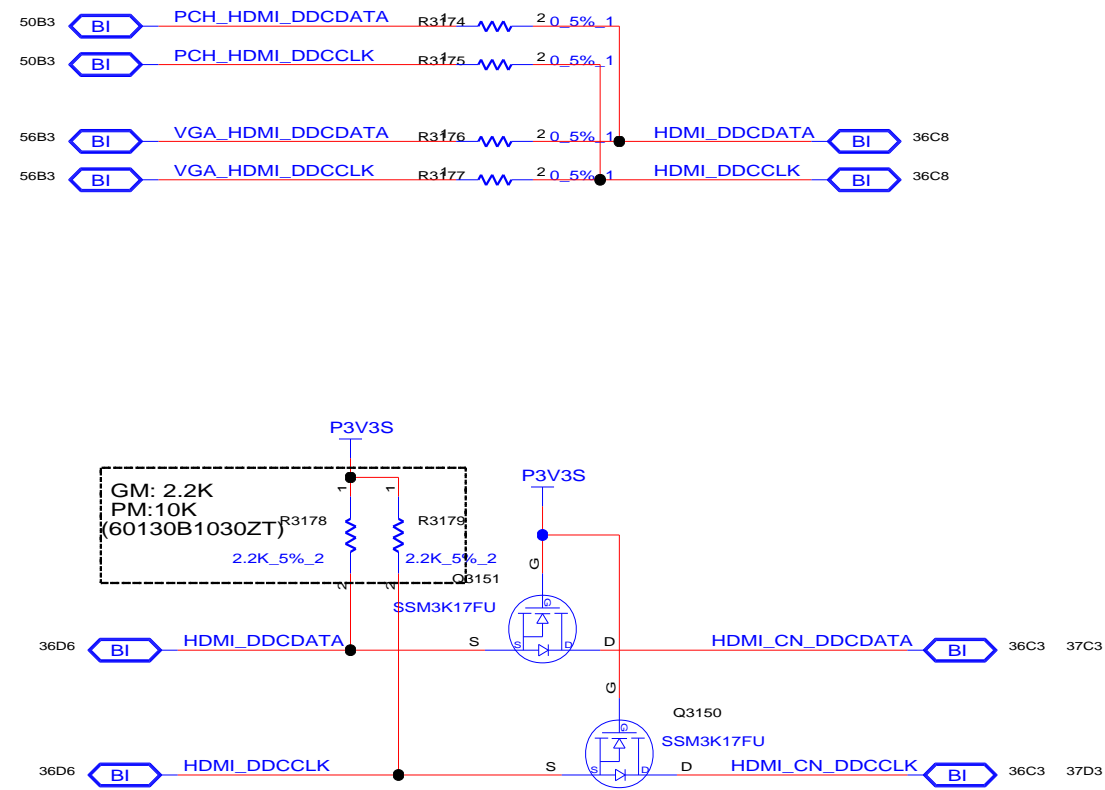
TITLE  
MODEL,PROJECT,FUNCTION  
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

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## REFERENCE 3150~3199(HDMI)



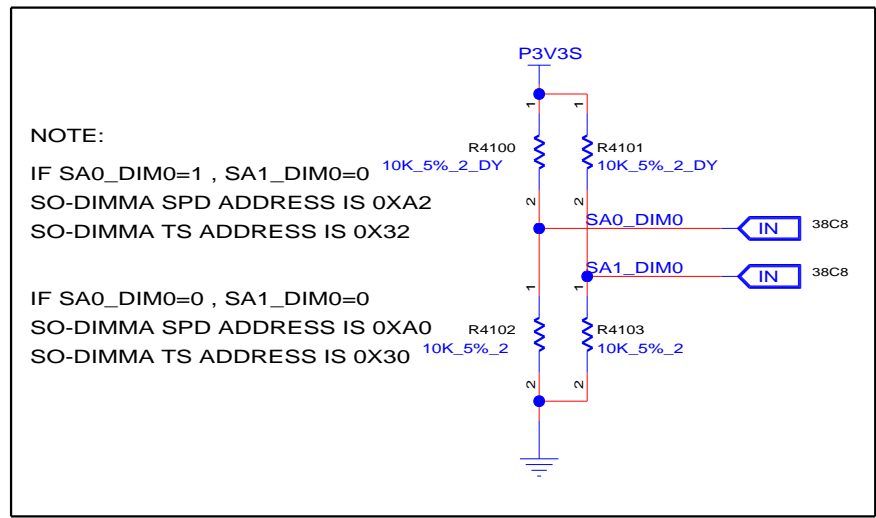
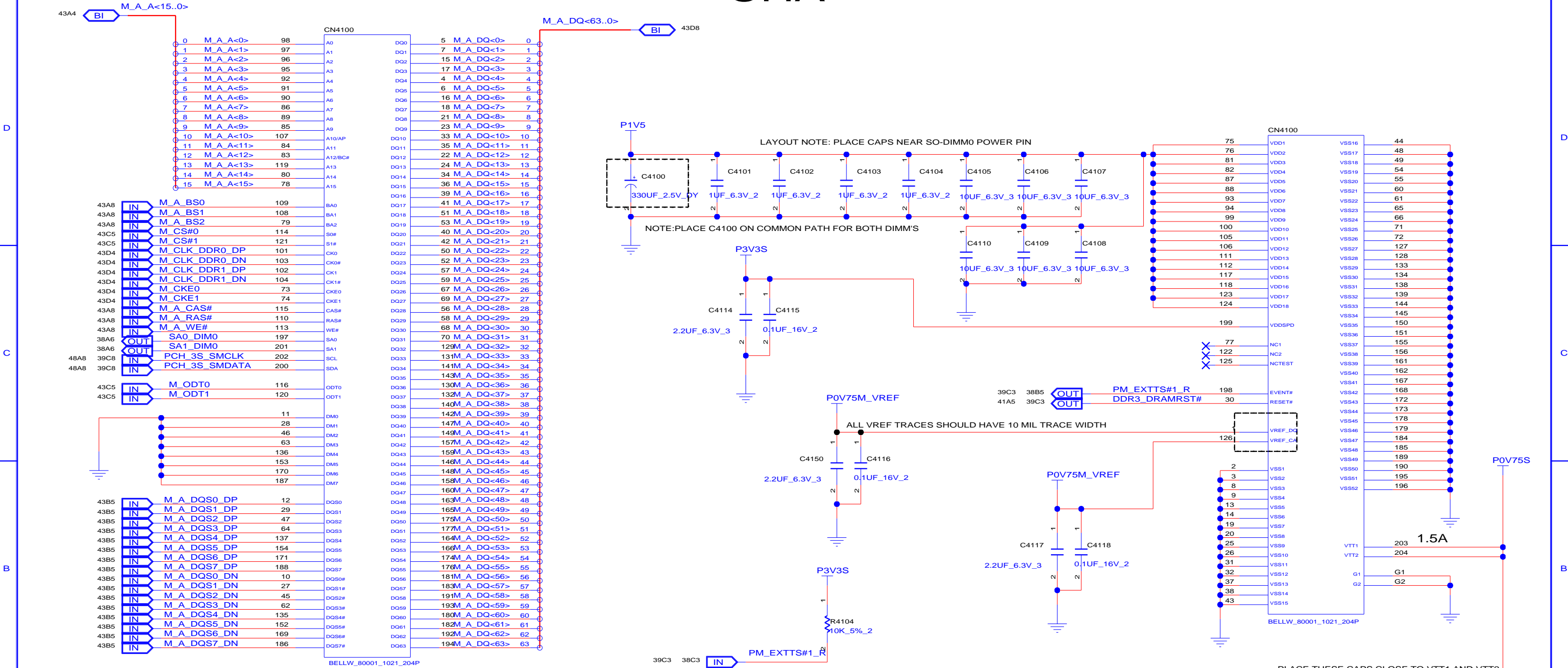
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TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	
AS	CS	1310xxxxx-0-0	



CHA

REFERENCE 4100~4299(DDR)

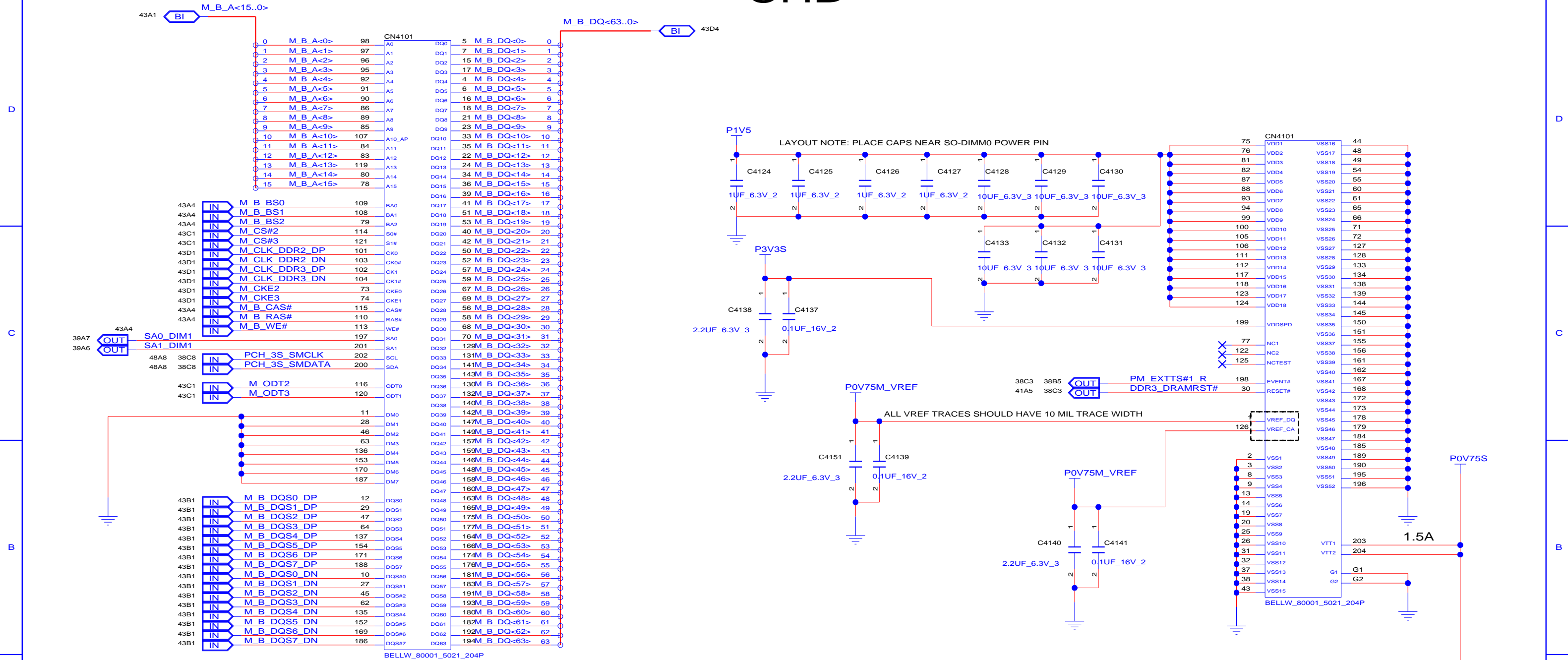


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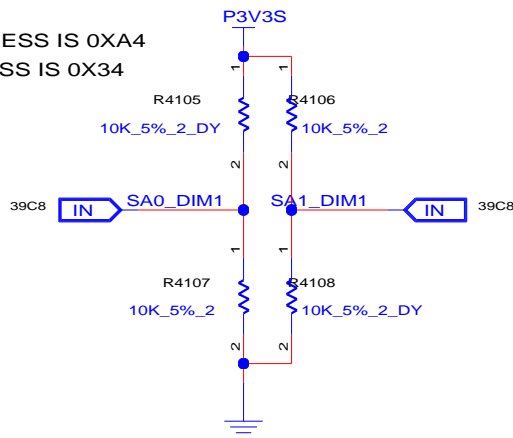
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REFERENCE 4100~4299(DDR)

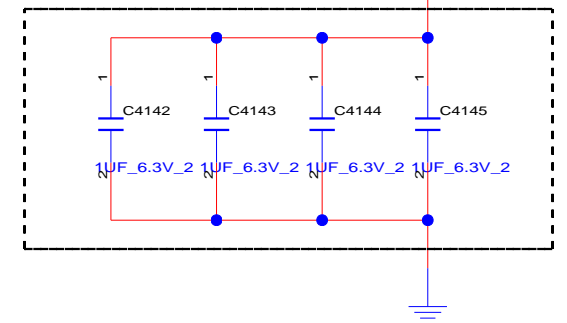
CHB



NOTE:  
SO-DIMMB SPD ADDRESS IS 0XA4  
SO-DIMMB TS ADDRESS IS 0X34



PLACE THESE CAPS CLOSE TO VTT1 AND VTT2

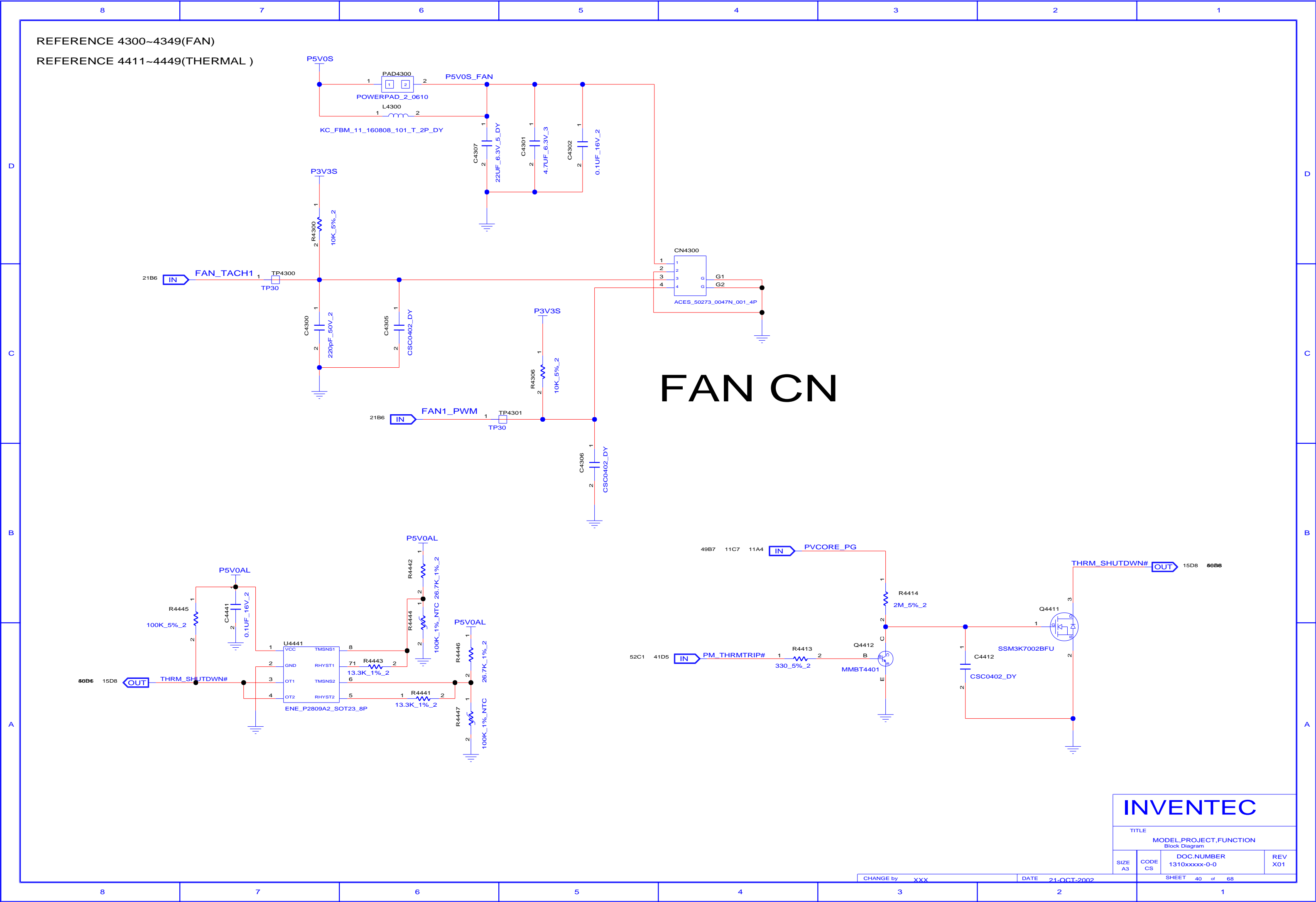


INVENTEC

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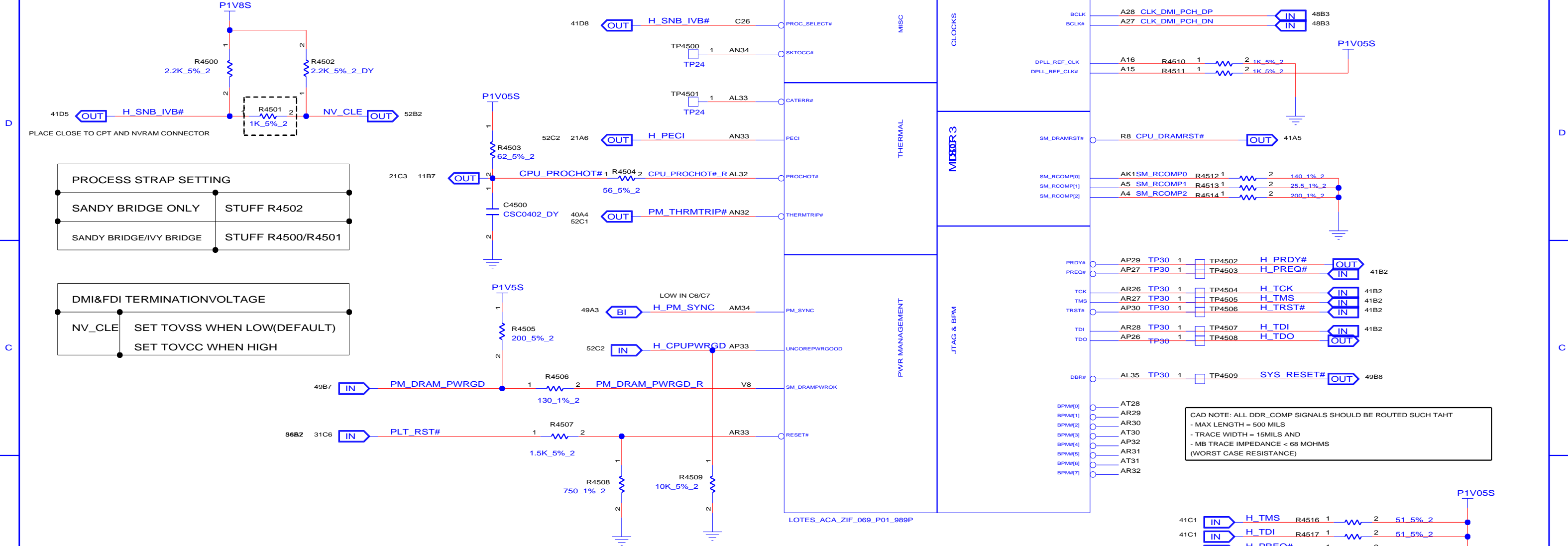
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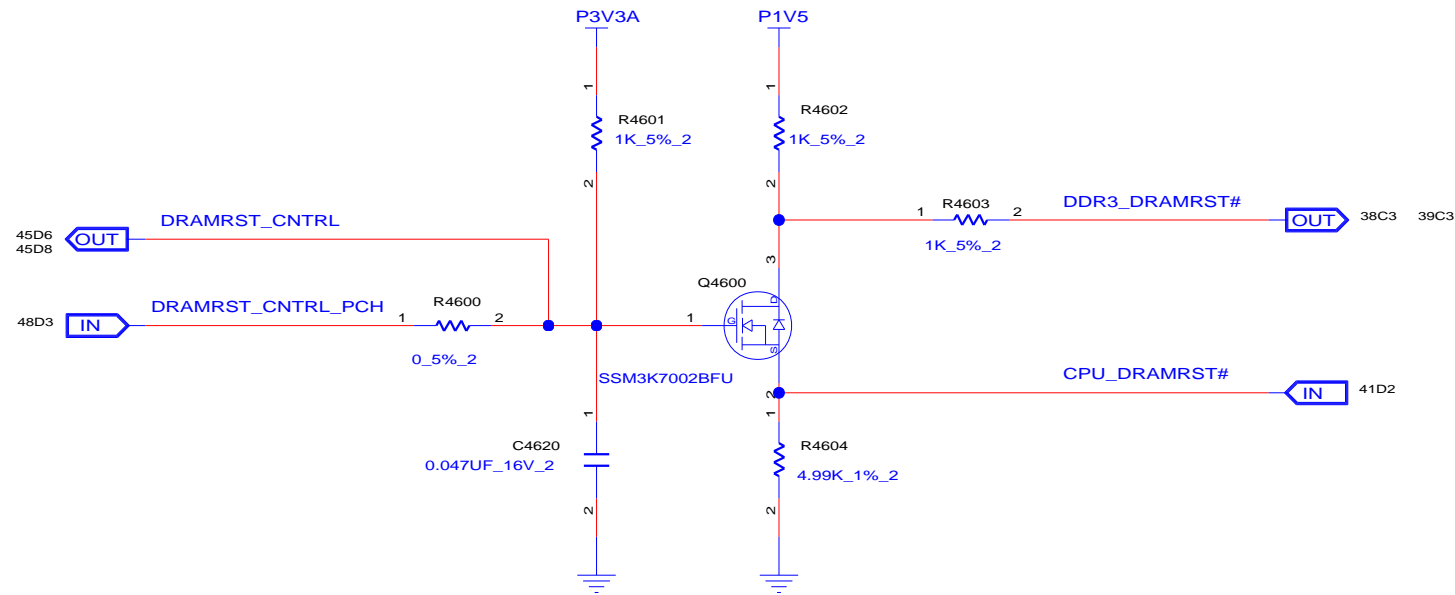




REFERENCE 4500~4699(CPU)



S3 CIRCUIT: DRAM\_RST# TO MEMORY SHOULD BE HIGH DURING S3



INVENTEC

TITLE  
MODEL,PROJECT,FUNCTION  
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

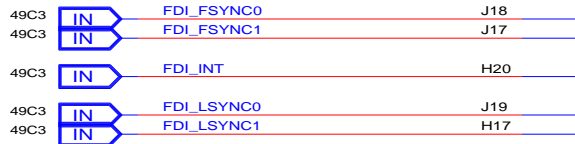
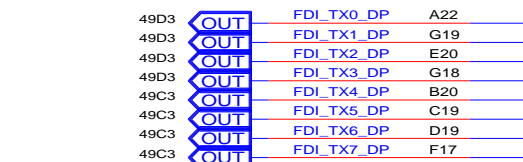
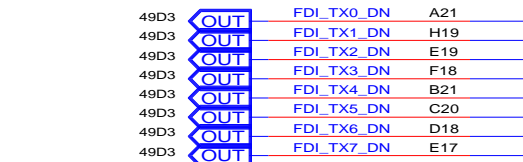
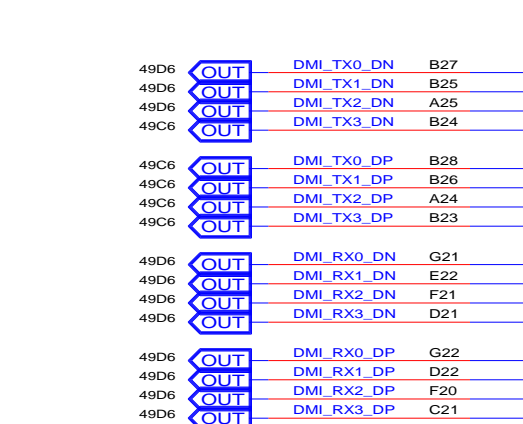
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REFERENCE 4500~4699(CPU)

P1V05S

R4521  
24.9\_1%\_2

CAD NOTE: DP\_COMPIO AND ICOMPO SIGNALS  
SHOULD BE SHORTED NEAR BALLS AND ROUTED WITH  
- TYPICAL IMPEDANCE < 25 MOHMS



CN4500

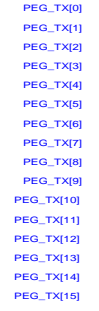
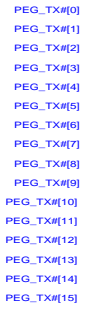
DMI

Intel(R) FDI

eDP

LOTES\_ACA\_ZIF\_069\_P01\_989P

PCI EXPRESS - GRAPHICS



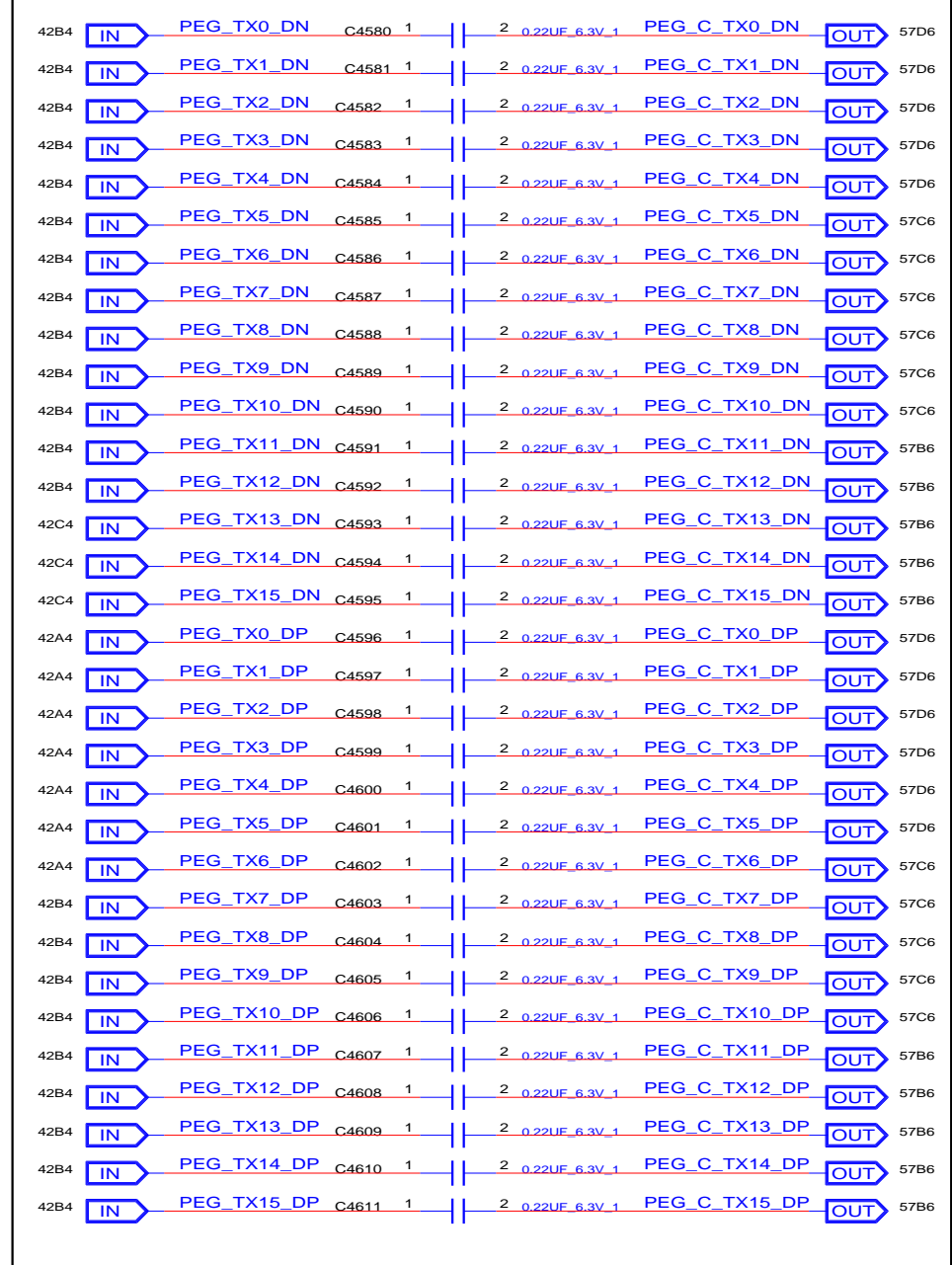
P1V05S

R4522  
24.9\_1%\_2

CAD NOTE: PEG\_ICOMPI AND RCOMPO SIGNALS  
SHOULD BE SHORTED AND ROUTED WITH  
- MAX LENGTH = 500 MILS  
- TYPICAL IMPEDANCE = 43 MOHMS

PEG\_ICOMPO SIGNALS SHOULD BE ROUTED WITH  
- MAX LENGTH = 500 MILS  
- TYPICAL IMPEDANCE = 14.5 MOHMS

CLOSE TO CPU



INVENTEC

TITLE  
MODEL,PROJECT,FUNCTION  
Block Diagram

SIZE A3 CODE CS DOC.NUMBER 1310xxxx-0-0 REV X01

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REFERENCE 4500~4699(CPU)

SOCKET,CPU,989P,TIN,3.0MM,STR,SMD,TR

D

C

B

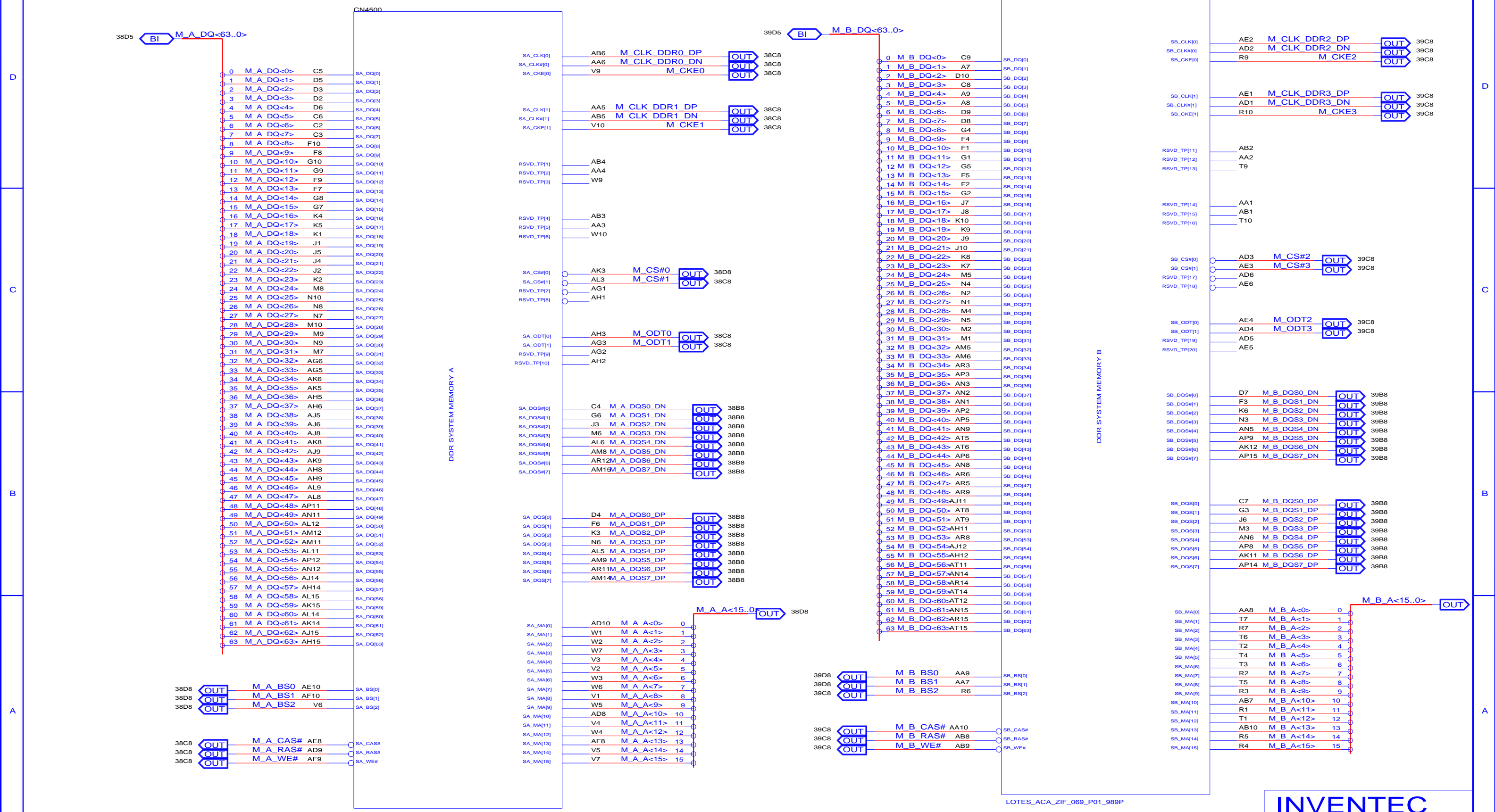
A

D

C

B

A

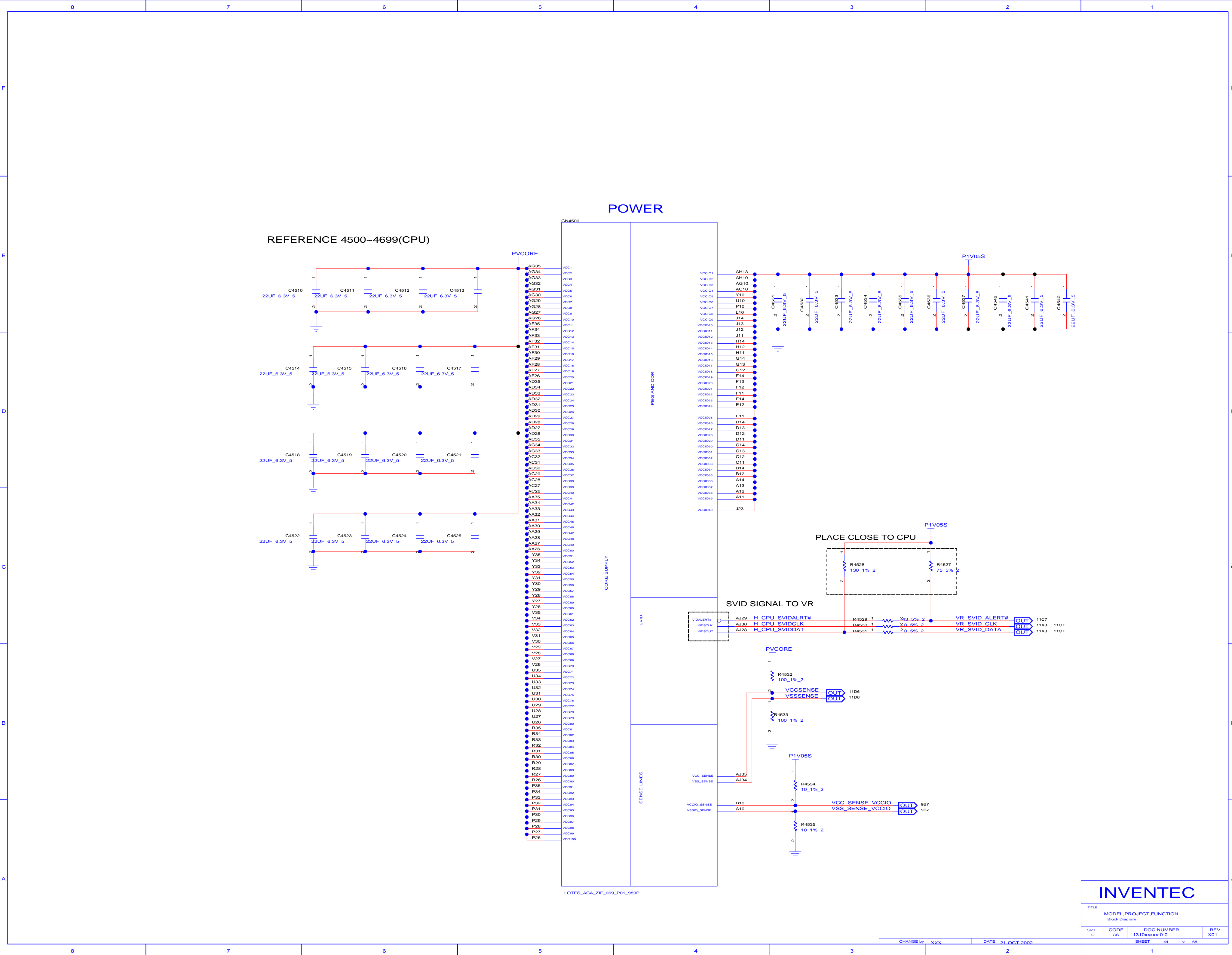


INVENTEC

TITLE  
MODEL,PROJECT,FUNCTION  
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

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POWER

REFERENCE 4500~4699(CPU)

PVCORE

CN4500

- AG35 VCC1
- AG34 VCC2
- AG33 VCC3
- AG32 VCC4
- AG31 VCC5
- AG30 VCC6
- AG29 VCC7
- AG28 VCC8
- AG27 VCC9
- AG26 VCC10
- AF35 VCC11
- AF34 VCC12
- AF33 VCC13
- AF32 VCC14
- AF31 VCC15
- AF30 VCC16
- AF29 VCC17
- AF28 VCC18
- AF27 VCC19
- AF26 VCC20
- AD35 VCC21
- AD34 VCC22
- AD33 VCC23
- AD32 VCC24
- AD31 VCC25
- AD30 VCC26
- AD29 VCC27
- AD28 VCC28
- AD27 VCC29
- AD26 VCC30
- AC35 VCC31
- AC34 VCC32
- AC33 VCC33
- AC32 VCC34
- AC31 VCC35
- AC30 VCC36
- AC29 VCC37
- AC28 VCC38
- AC27 VCC39
- AC26 VCC40
- AA35 VCC41
- AA34 VCC42
- AA33 VCC43
- AA32 VCC44
- AA31 VCC45
- AA30 VCC46
- AA29 VCC47
- AA28 VCC48
- AA27 VCC49
- AA26 VCC50
- Y35 VCC51
- Y34 VCC52
- Y33 VCC53
- Y32 VCC54
- Y31 VCC55
- Y30 VCC56
- Y29 VCC57
- Y28 VCC58
- Y27 VCC59
- Y26 VCC60
- V35 VCC61
- V34 VCC62
- V33 VCC63
- V32 VCC64
- V31 VCC65
- V30 VCC66
- V29 VCC67
- V28 VCC68
- V27 VCC69
- V26 VCC70
- U35 VCC71
- U34 VCC72
- U33 VCC73
- U32 VCC74
- U31 VCC75
- U30 VCC76
- U29 VCC77
- U28 VCC78
- U27 VCC79
- U26 VCC80
- R35 VCC81
- R34 VCC82
- R33 VCC83
- R32 VCC84
- R31 VCC85
- R30 VCC86
- R29 VCC87
- R28 VCC88
- R27 VCC89
- R26 VCC90
- P34 VCC91
- P33 VCC92
- P32 VCC93
- P31 VCC94
- P30 VCC95
- P29 VCC96
- P28 VCC97
- P27 VCC98
- P26 VCC100

PEG AND DDR

CORE SUPPLY

SVID

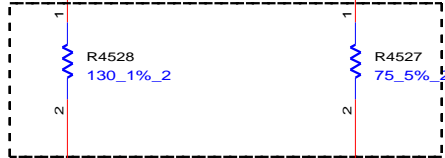
SENSE LINES

LOTES\_ACA\_ZIF\_069\_P01\_989P

PLACE CLOSE TO CPU

SVID SIGNAL TO VR

P1V05S



PVCORE

VCCSENSE

VSSSENSE

P1V05S

VCC\_SENSE\_VCCIO

VSS\_SENSE\_VCCIO

INVENTEC

TITLE  
MODEL,PROJECT,FUNCTION  
Block Diagram

SIZE	CODE	DOC NUMBER	REV
C	CS	1310XXXX-0-0	X01

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POWER

SENSE LINES

VREF

DDR3 -1.5V RAILS

1.8V RAIL

MISC

GRAPHICS

1.8V RAIL

LOTES\_ACA\_ZIF\_069\_P01\_989P

NOTE : DDR\_WR\_VREF SHOULD HAVE 20/20 MIL WHEREVER POSSIBLE

INVENTEC

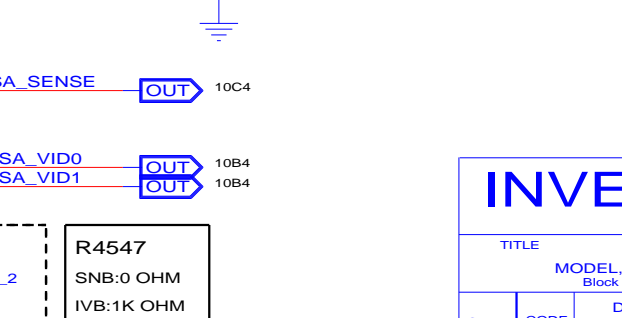
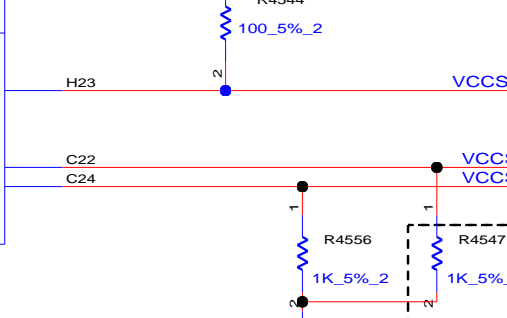
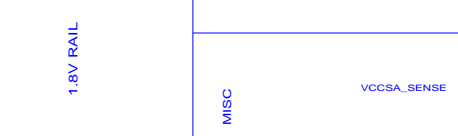
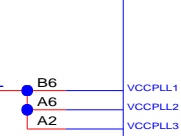
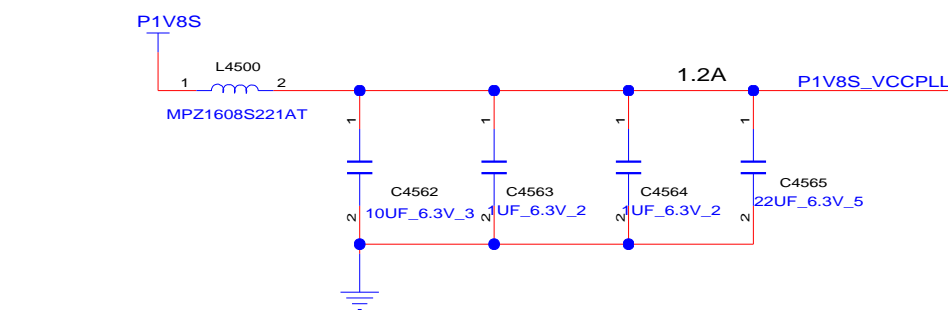
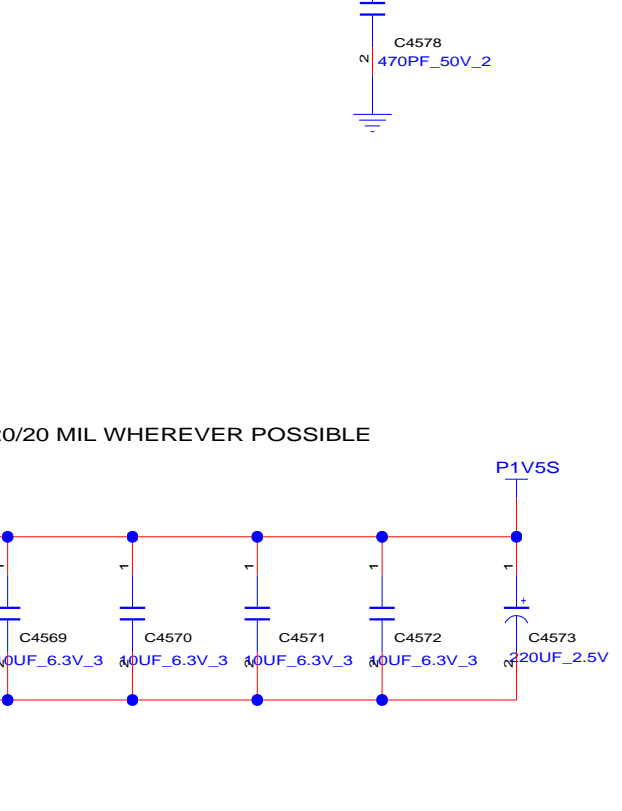
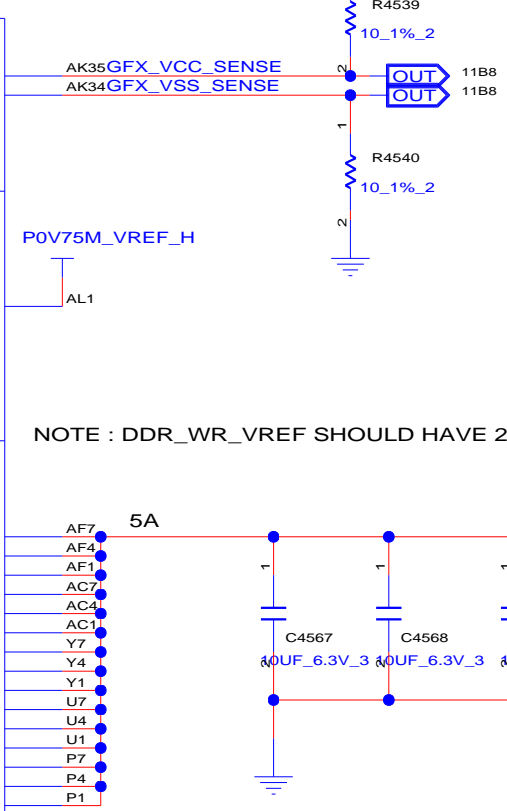
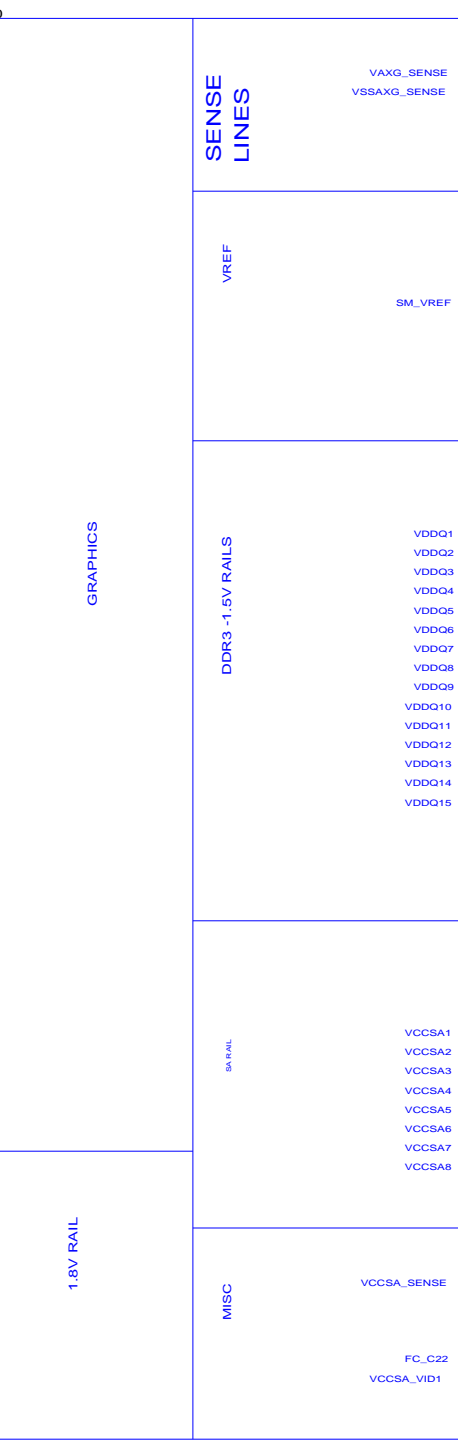
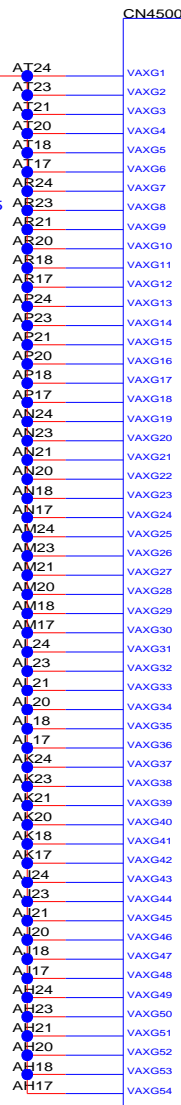
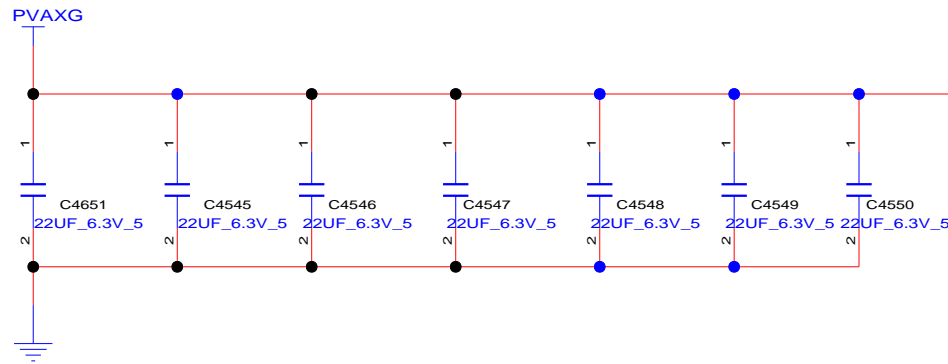
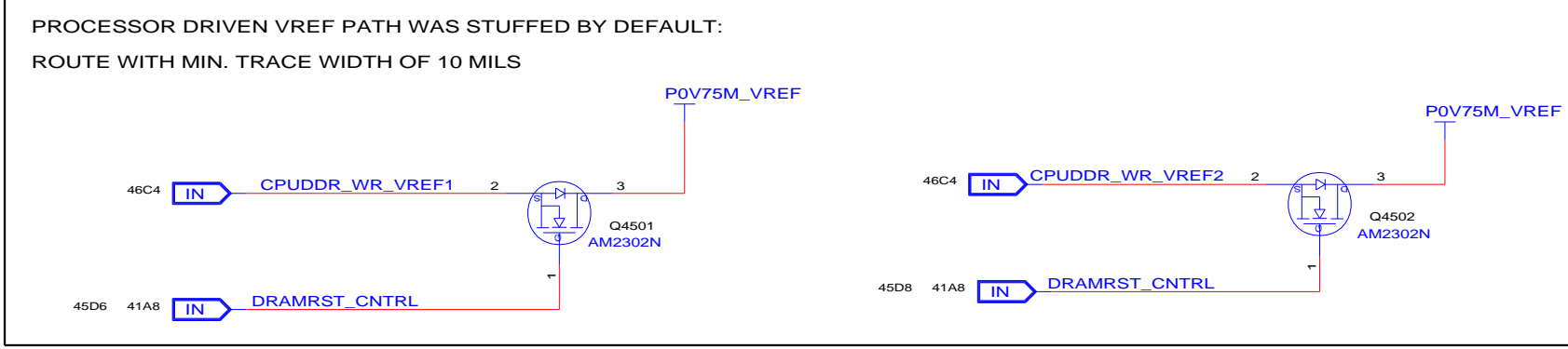
TITLE MODEL,PROJECT,FUNCTION  
Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
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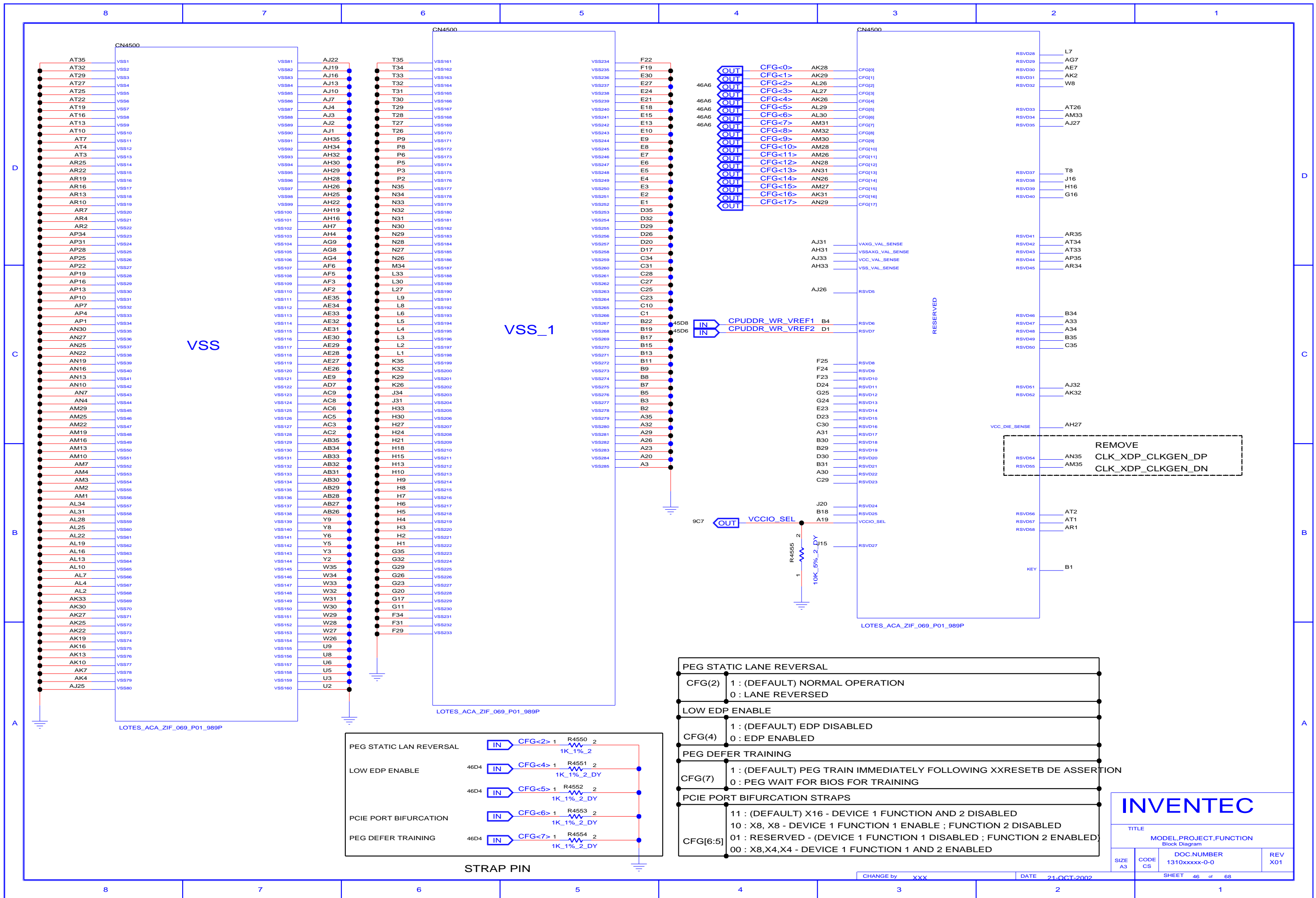
SHEET 45 of 68

DATE 21-OCT-2002

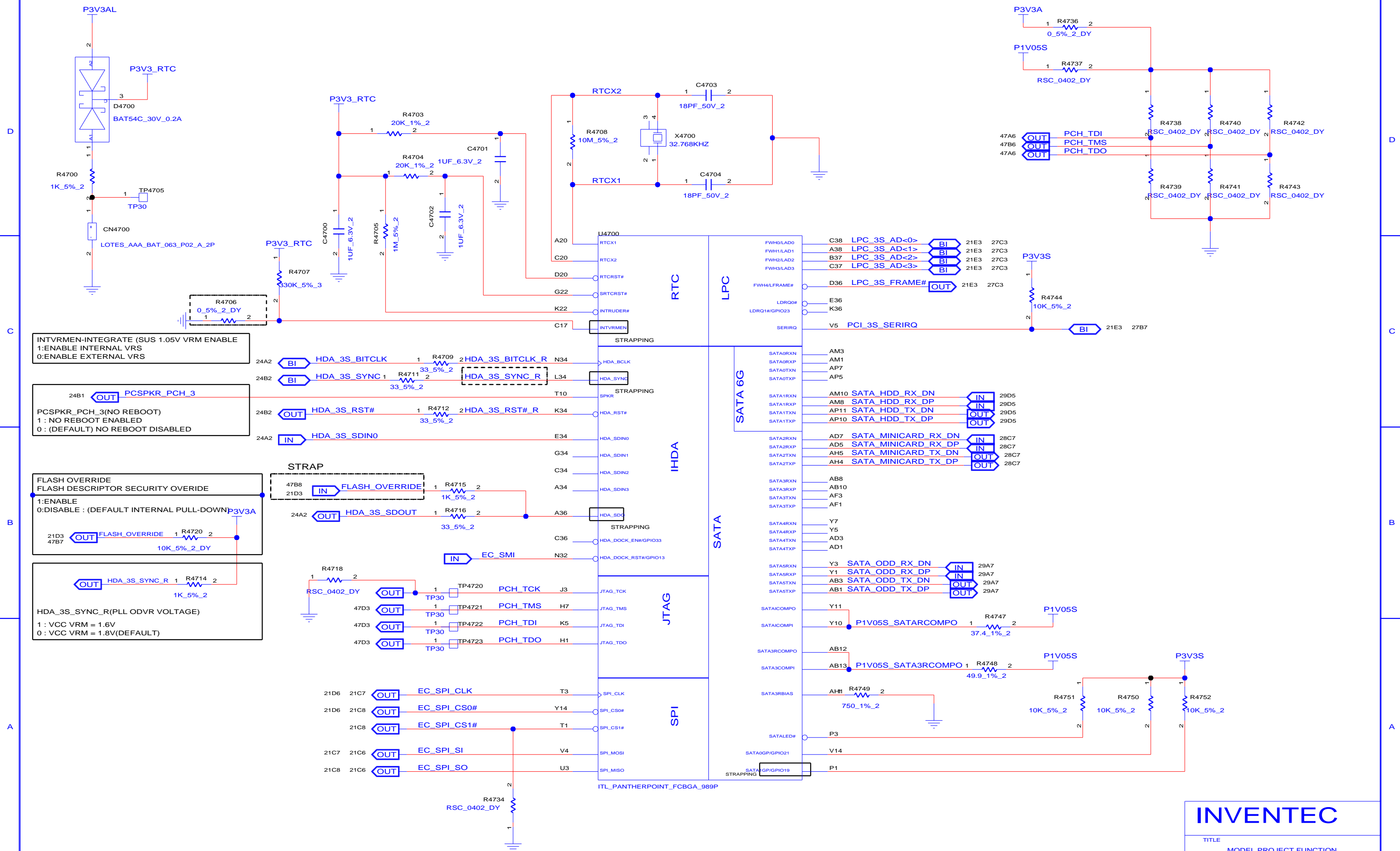
CHANGE by XXX







REFERENCE 4700~4949(PCH)



# INVENTEC

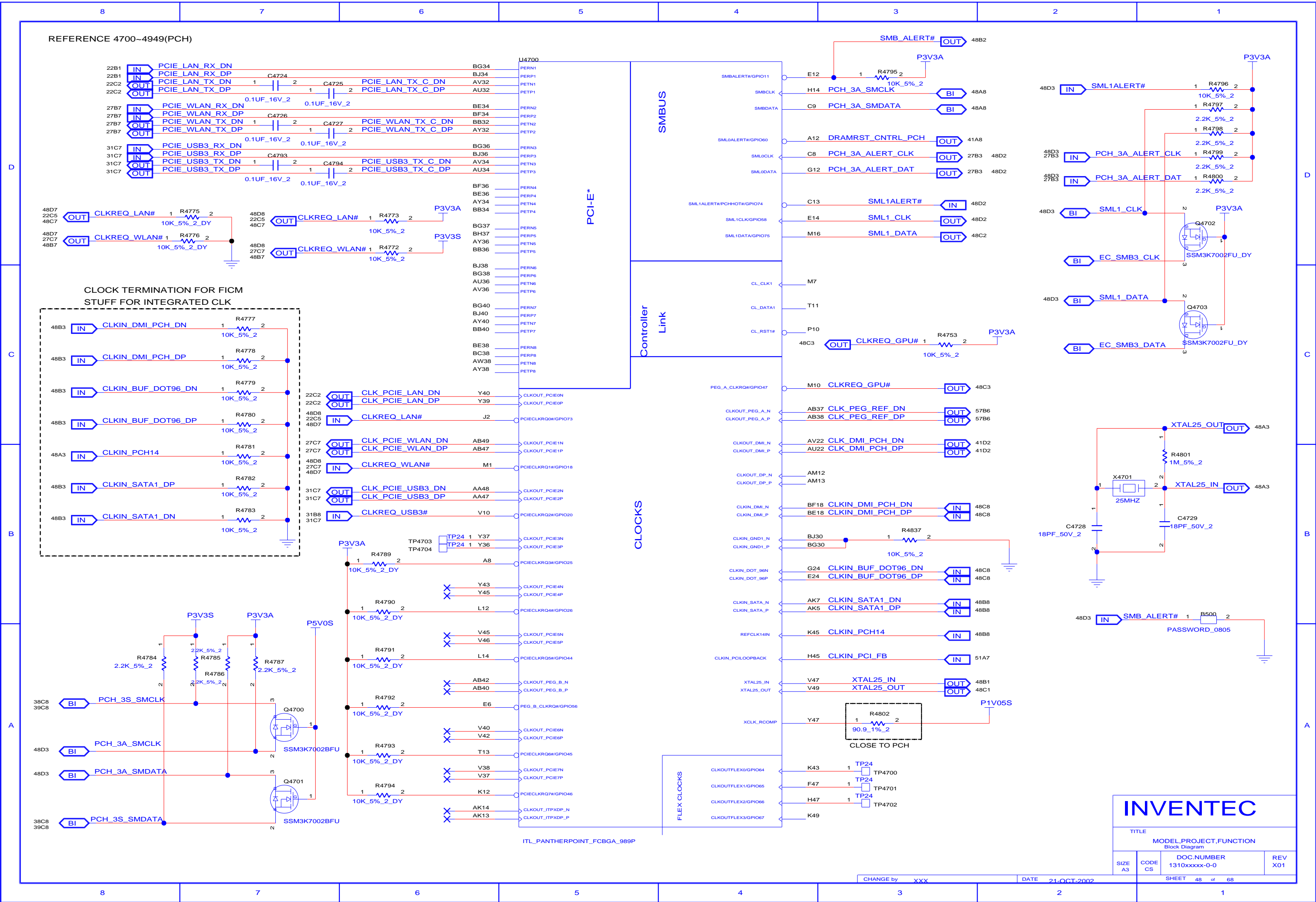
TITLE \_\_\_\_\_

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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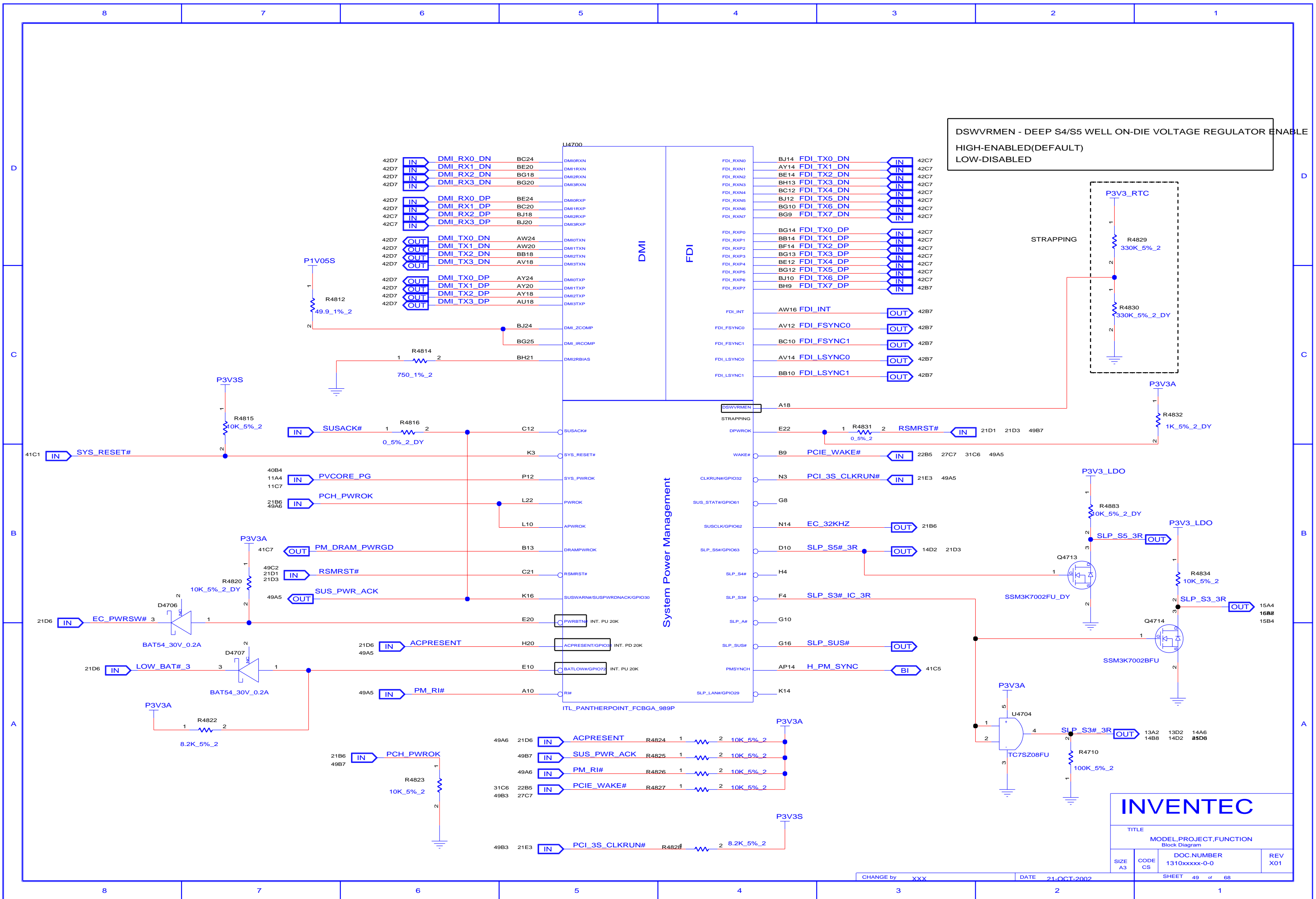
A3	C6		
SHEET 47 of 68			

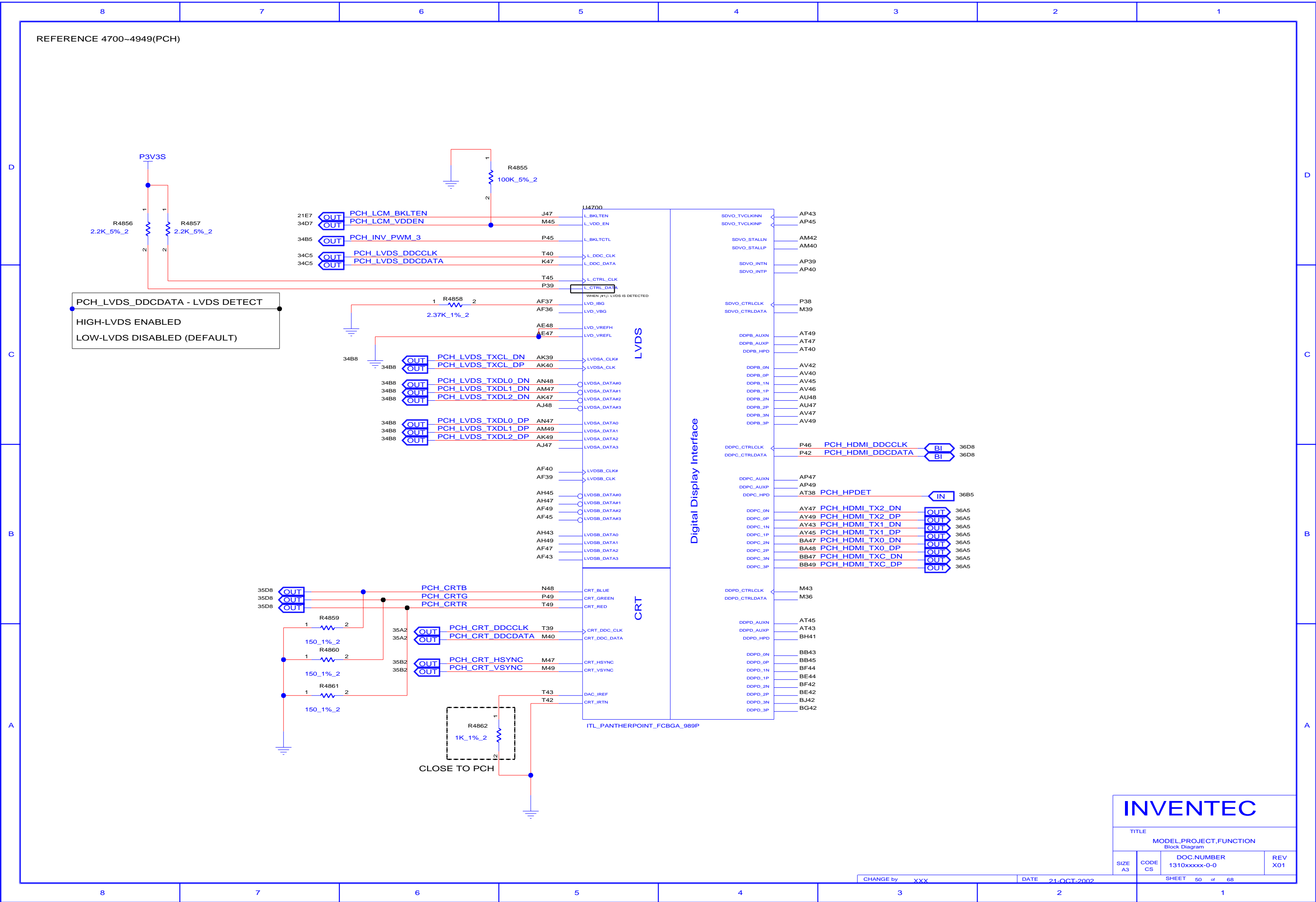
CHANGE by	XXX	DATE	21-OCT-2002
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SHEET 47 of 68



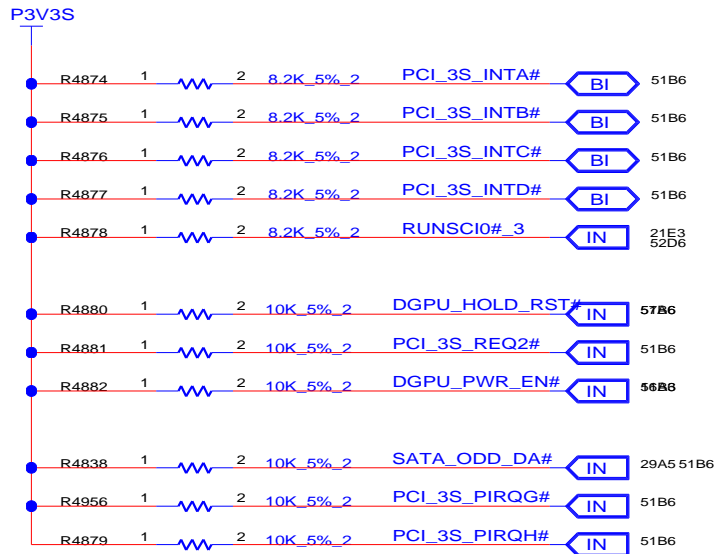




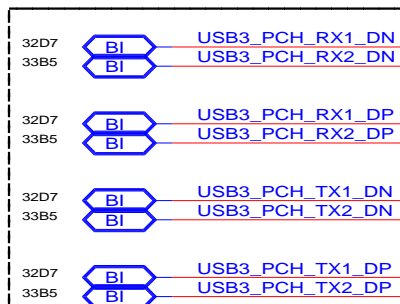


REFERENCE 4700~4949(PCH)

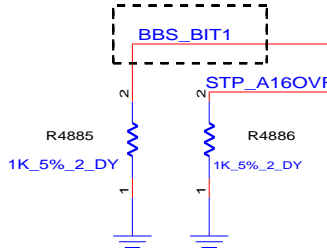
GPIO51 BBS_BIT1	GPIO19 BBS_BIT0	BOOT BIOS DESTINATION
0	1	RESERVED(NAND)
1	0	-----
1	1	SPI (DEFAULT)
0	0	LPC



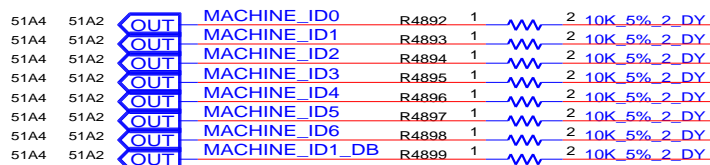
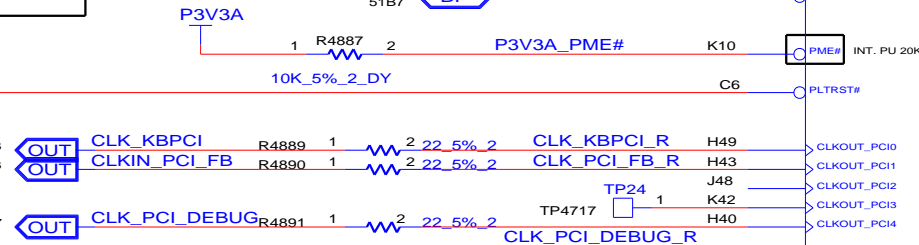
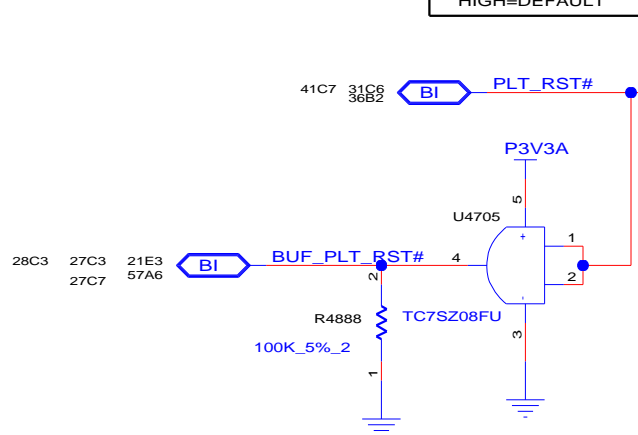
ROUTE WITH 90 OHMS IMPEDANCE  
TOTAL LENGTH NO LONGER THAN 11 INCHES



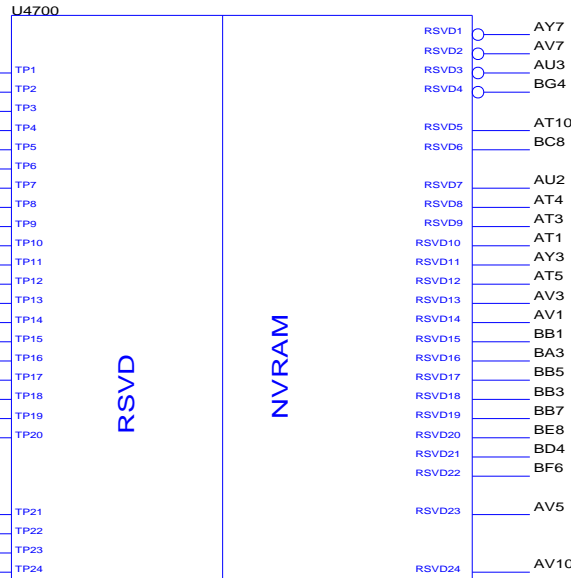
BBS STRAPING



LOW=A16 SWAP OVERRIDE  
STP\_A16OVR  
TOP-BLOCK SWAP OVERRIDE  
HIGH=DEFAULT



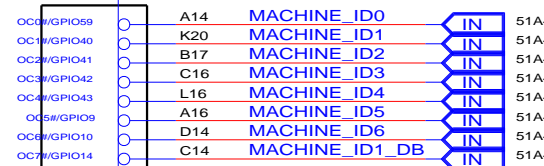
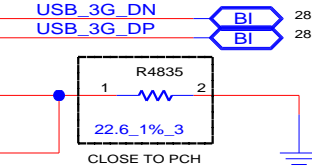
NOTE:10K\_5%(60130B1030ZT)



NOTE:  
USB2.0/3.0 COMBO-USB2.0 PORT 0,1 MAPPED USB3.0 PORT 1,2



CARD READER  
WLAN  
WEBCAM



TO BE USED AS GPIO

NOTE:10K\_5%(60130B1030ZT)

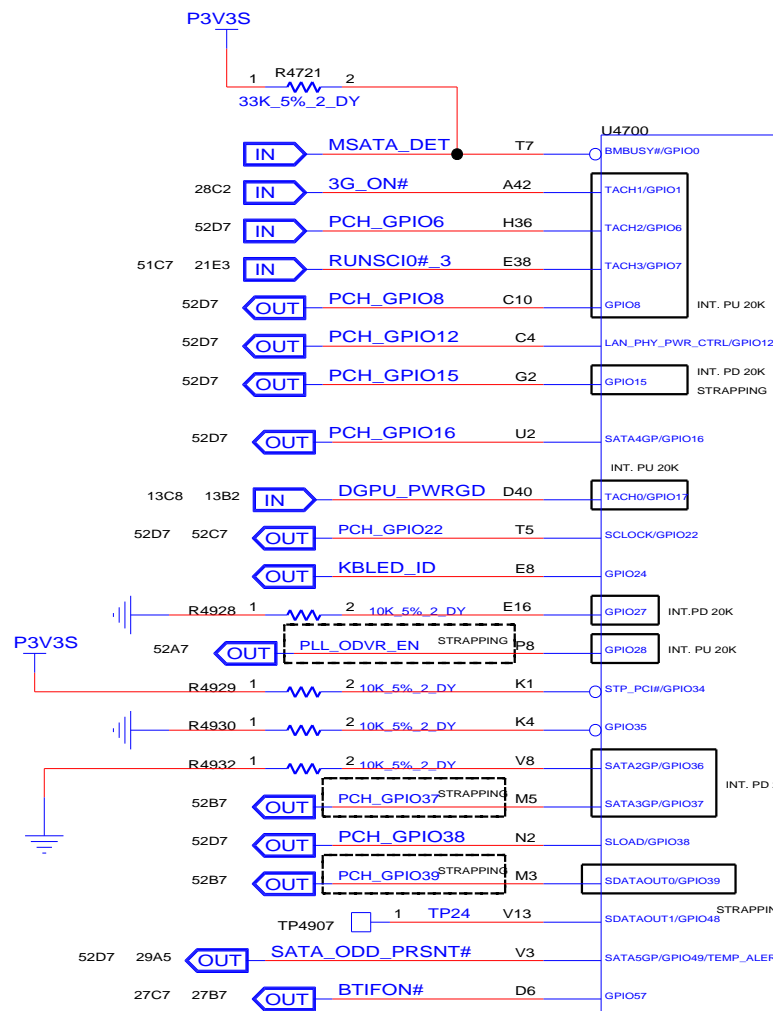
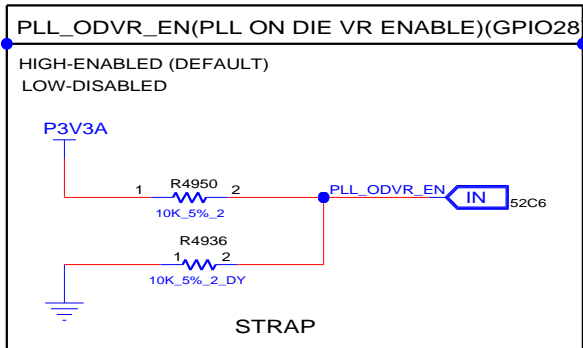
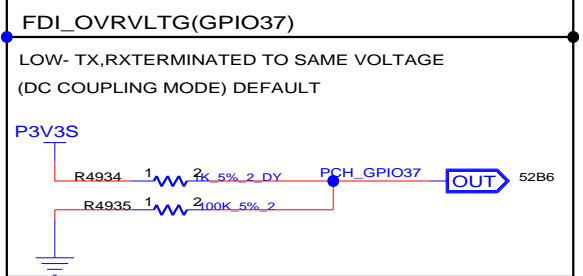
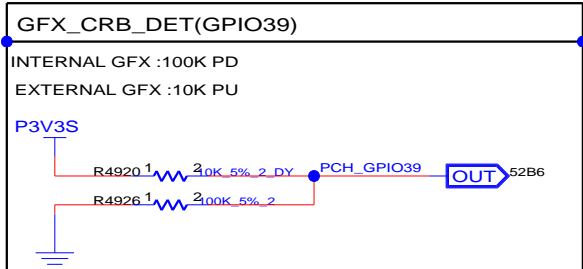
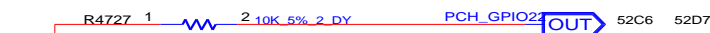
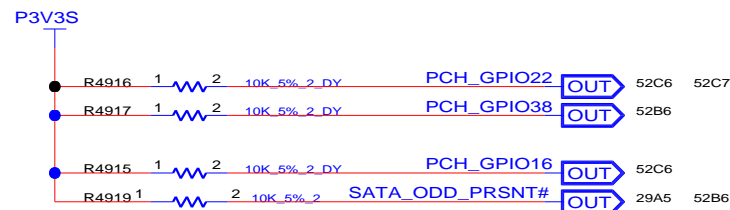
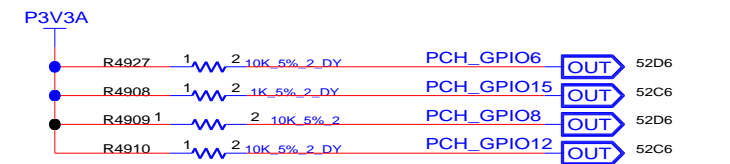
INVENTEC

TITLE  
MODEL,PROJECT,FUNCTION  
Block Diagram

SIZE A3 CODE CS DOC.NUMBER 1310xxxx-0-0 REV X01

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REFERENCE 4700~4949(PCH)



GPIO

NCTF

A4 VSS\_NCTF\_1

A44 VSS\_NCTF\_2

A45 VSS\_NCTF\_3

A46 VSS\_NCTF\_4

A5 VSS\_NCTF\_5

A6 VSS\_NCTF\_6

B3 VSS\_NCTF\_7

B47 VSS\_NCTF\_8

BD1 VSS\_NCTF\_9

BD49 VSS\_NCTF\_10

BE1 VSS\_NCTF\_11

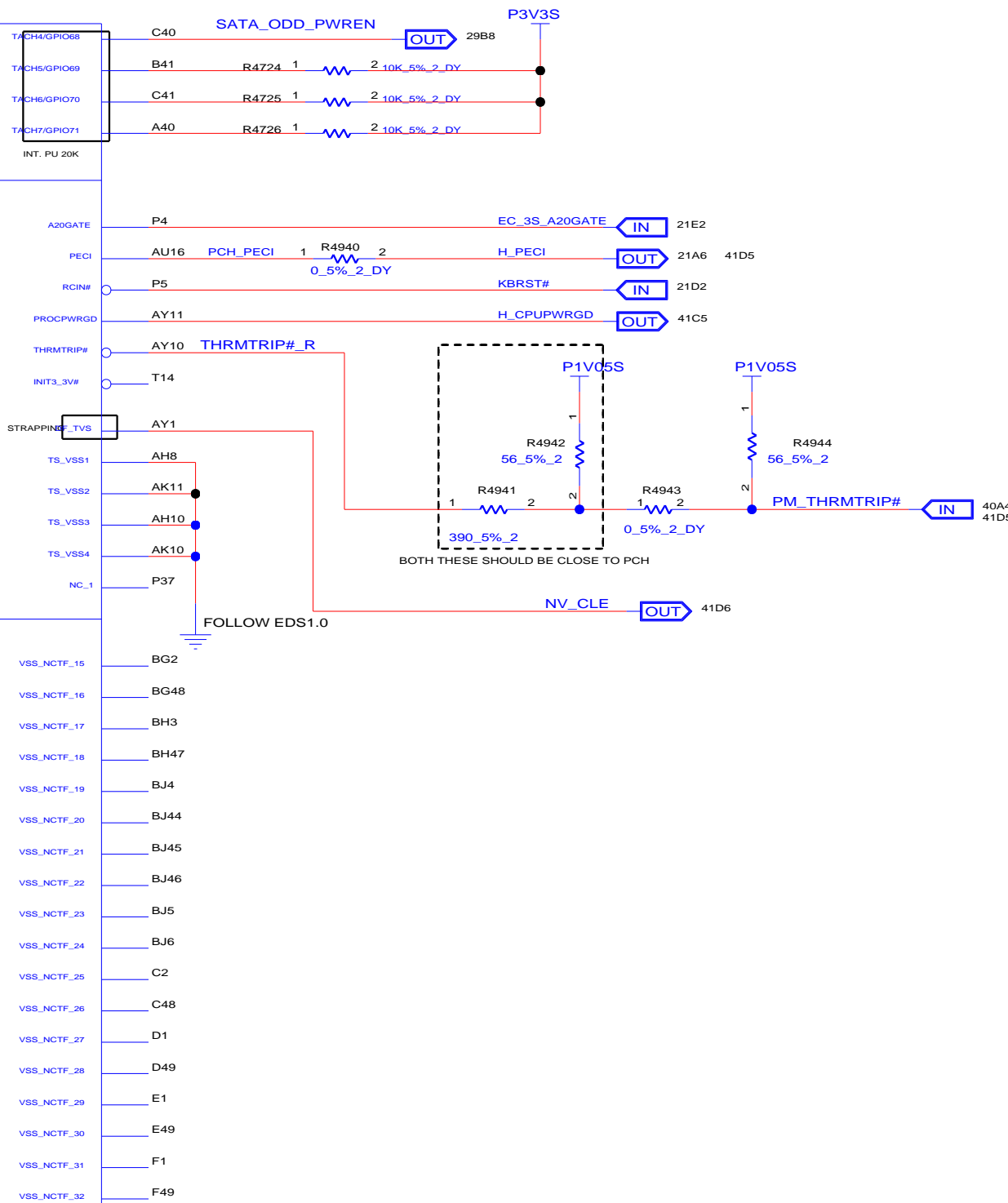
BE49 VSS\_NCTF\_12

BF1 VSS\_NCTF\_13

BF49 VSS\_NCTF\_14

ITL\_PANTHERPOINT\_FCBGA\_989P

CPU/MISC



INVENTEC

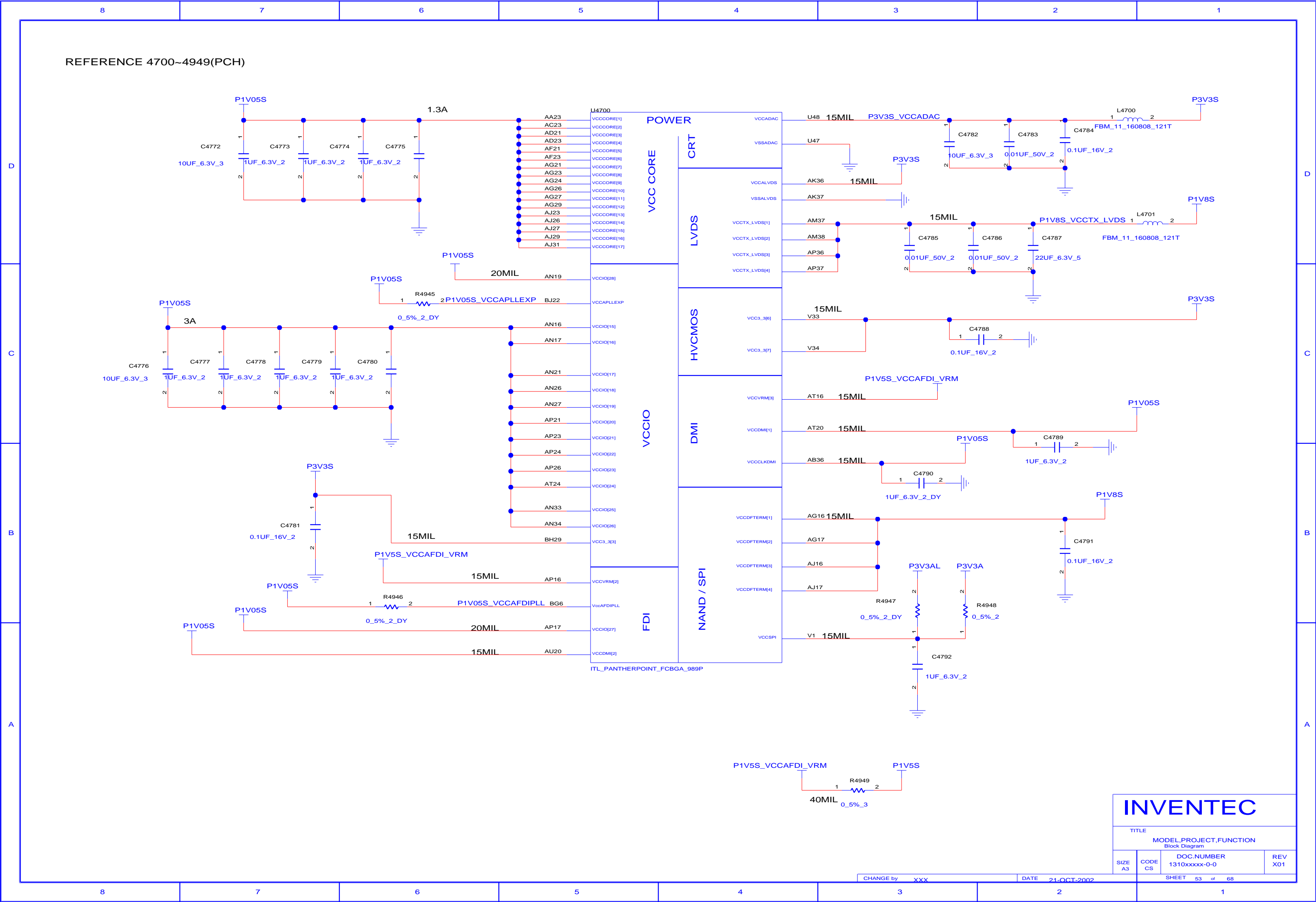
TITLE

MODEL,PROJECT,FUNCTION

Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
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CHANGE by XXX DATE 21.OCT-2002 SHEET 52 of 68

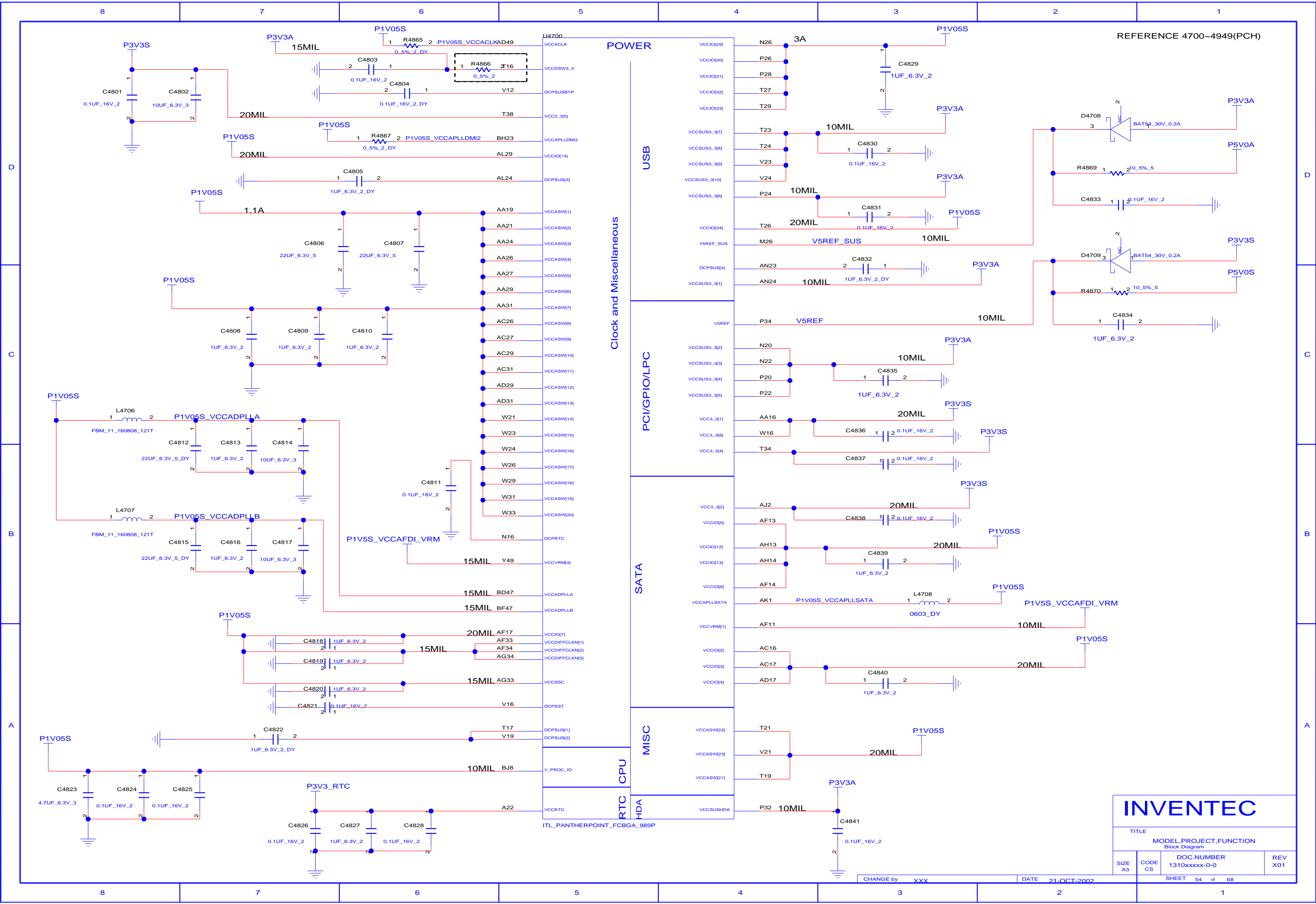


INVENTEC

TITLE  
MODEL,PROJECT,FUNCTION  
Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
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CHANGE by XXX DATE 21-OCT-2002 SHEET 53 of 68

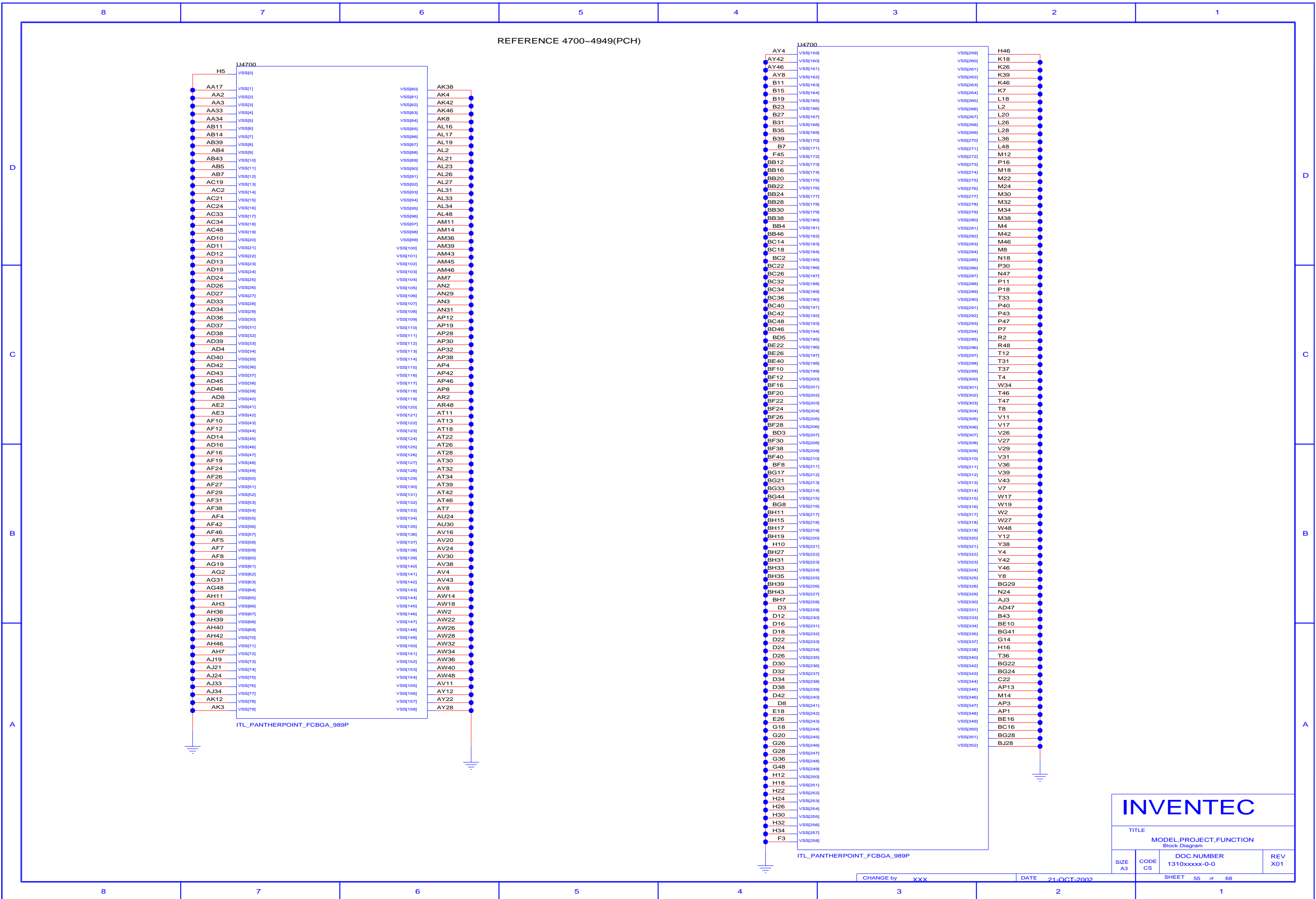


INVENTEC

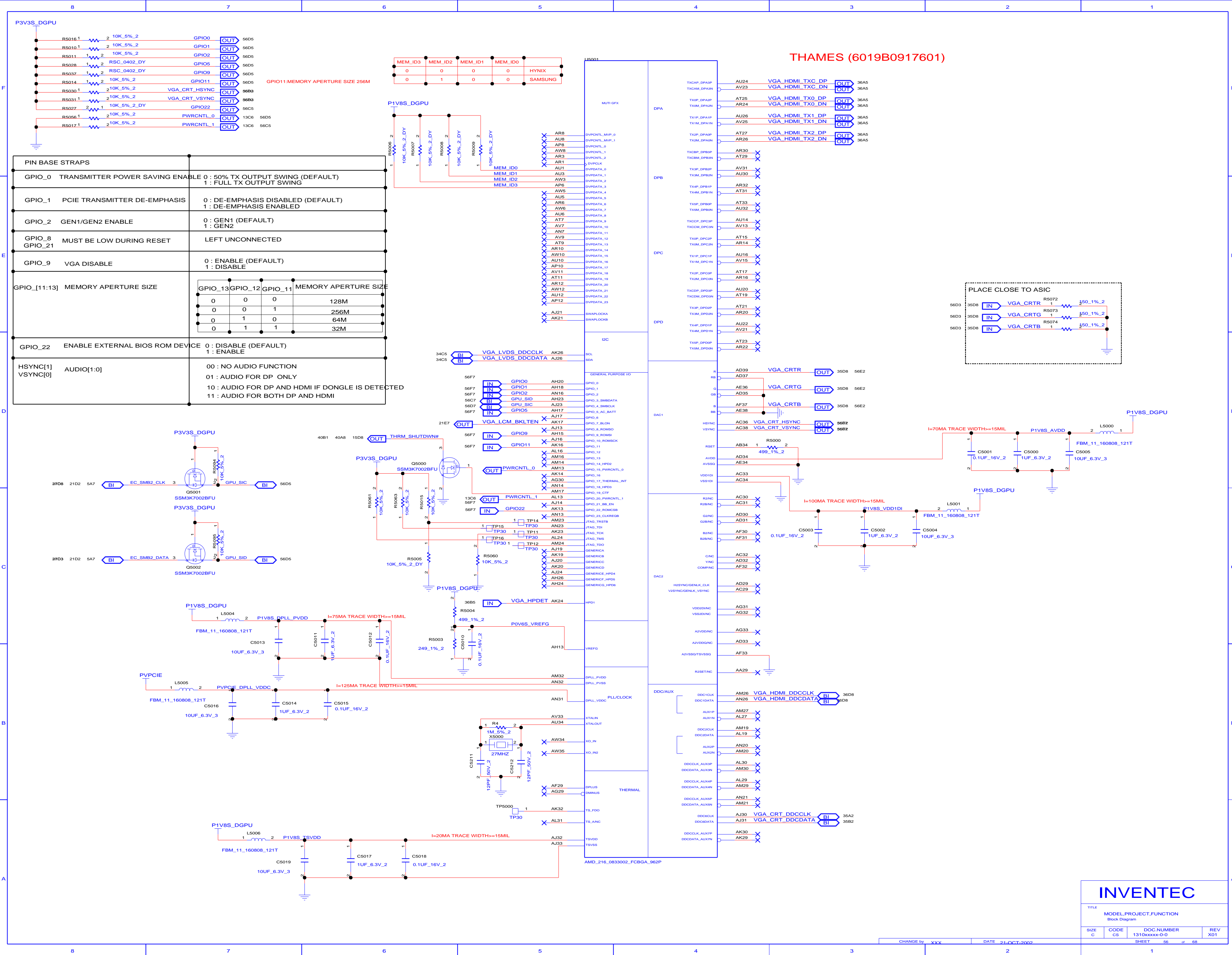
TITLE  
MODEL,PROJECT,FUNCTION  
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

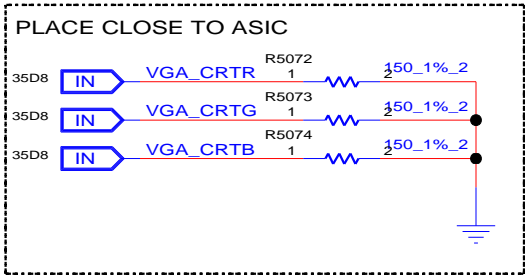
CHANGE by XXX DATE 21-OCT-2002 SHEET 54 of 68







PIN BASE STRAPS	
GPIO_0	TRANSMITTER POWER SAVING ENABLE 0 : 50% TX OUTPUT SWING (DEFAULT) 1 : FULL TX OUTPUT SWING
GPIO_1	PCIE TRANSMITTER DE-EMPHASIS 0 : DE-EMPHASIS DISABLED (DEFAULT) 1 : DE-EMPHASIS ENABLED
GPIO_2	GEN1/GEN2 ENABLE 0 : GEN1 (DEFAULT) 1 : GEN2
GPIO_8 GPIO_21	MUST BE LOW DURING RESET LEFT UNCONNECTED
GPIO_9	VGA DISABLE 0 : ENABLE (DEFAULT) 1 : DISABLE
GPIO_[11:13]	MEMORY APERTURE SIZE GPIO_13GPIO_12GPIO_11MEMORY APERTURE SIZE 000128M 001256M 01064M 01132M
GPIO_22	ENABLE EXTERNAL BIOS ROM DEVICE 0 : DISABLE (DEFAULT) 1 : ENABLE
HSYNC[1] VSYNC[0]	AUDIO[1:0] 00 : NO AUDIO FUNCTION 01 : AUDIO FOR DP ONLY 10 : AUDIO FOR DP AND HDMI IF DONGLE IS DETECTED 11 : AUDIO FOR BOTH DP AND HDMI

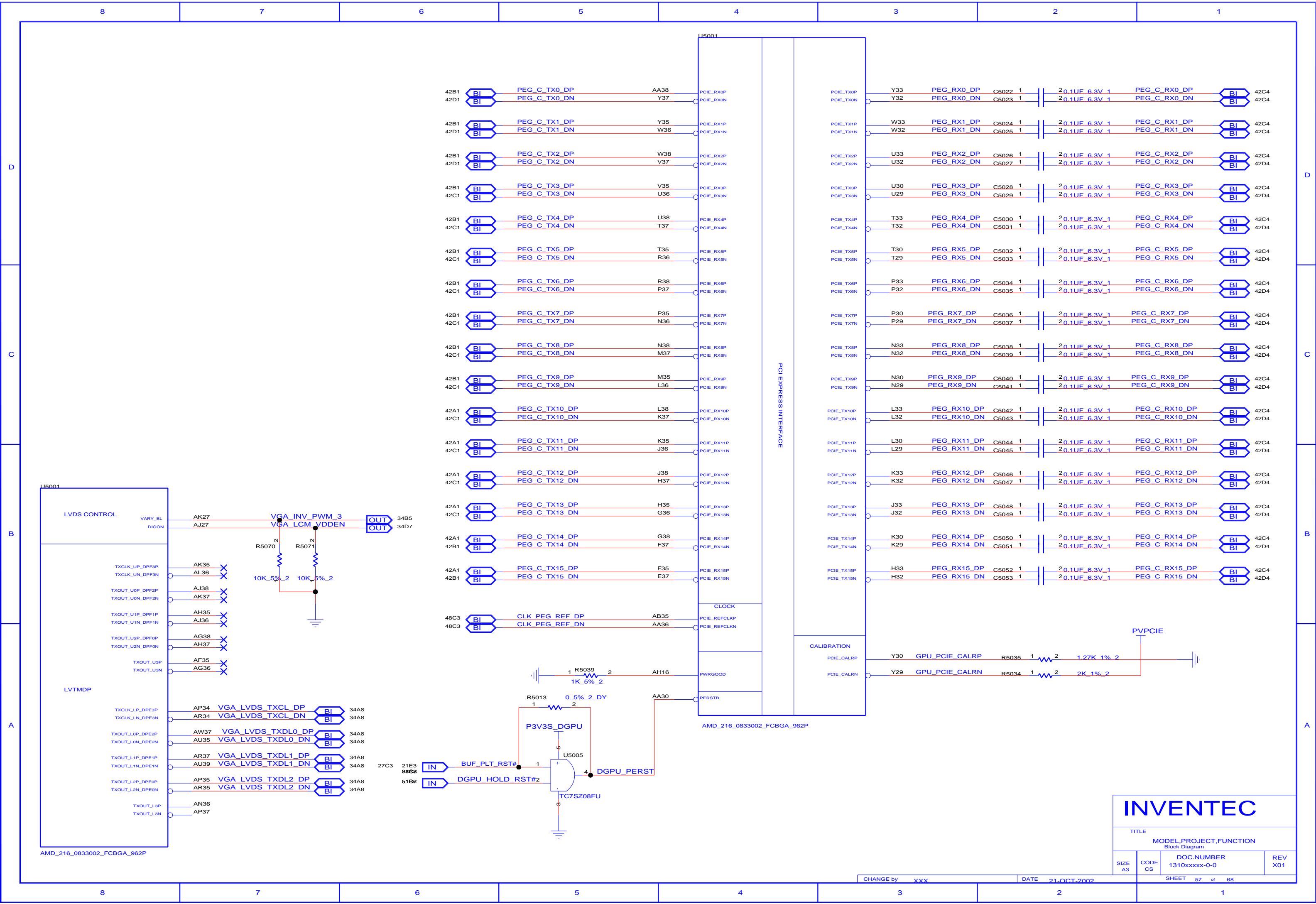


INVENTEC

TITLE			
MODEL_PROJECT_FUNCTION Block Diagram			
SIZE C	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SHEET 56 of 68			

CHANGE by xxx DATE 21.OCT.2002



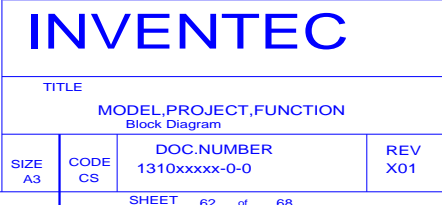




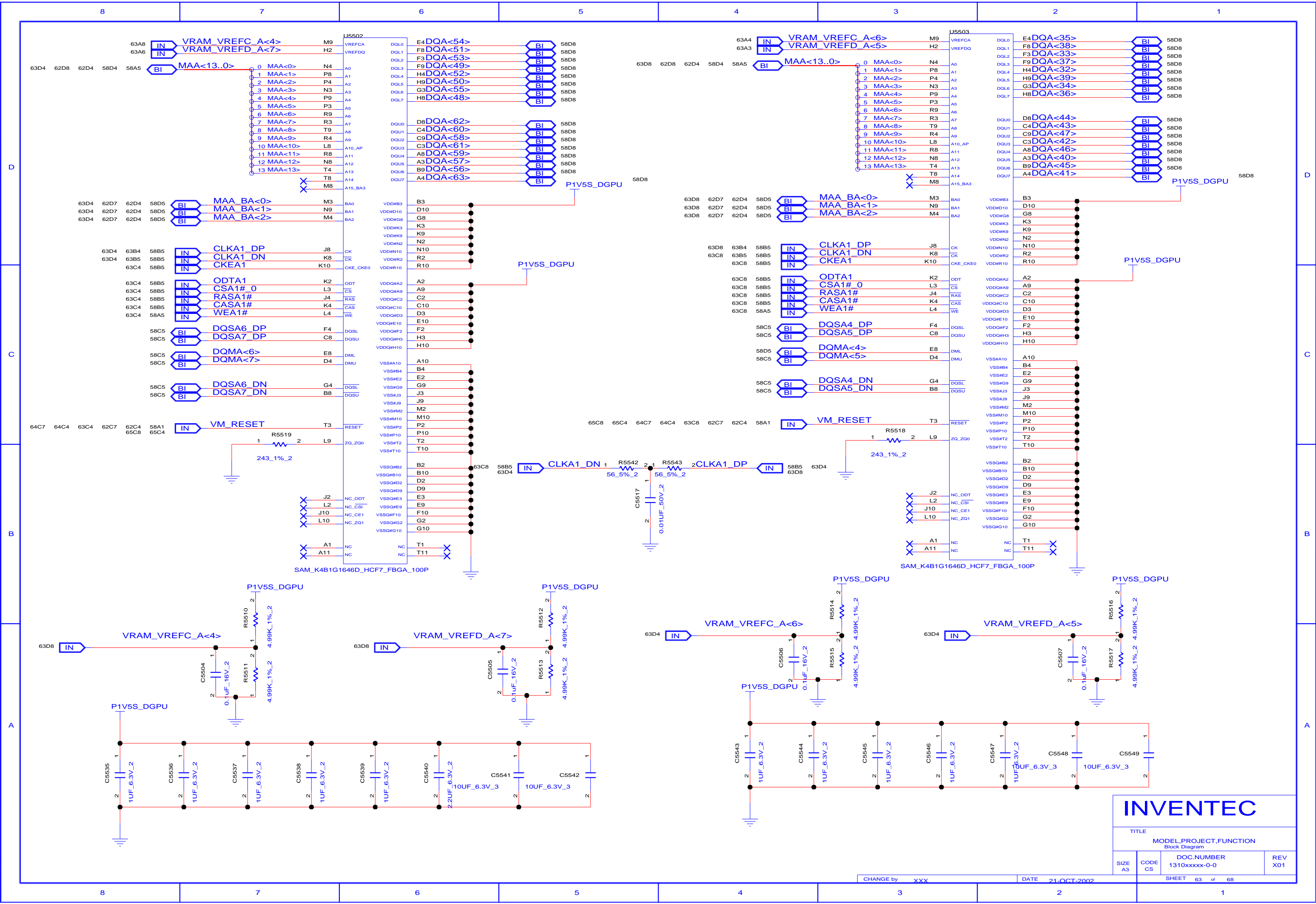












INVENTEC

TITLE

MODEL,PROJECT,FUNCTION  
Block Diagram

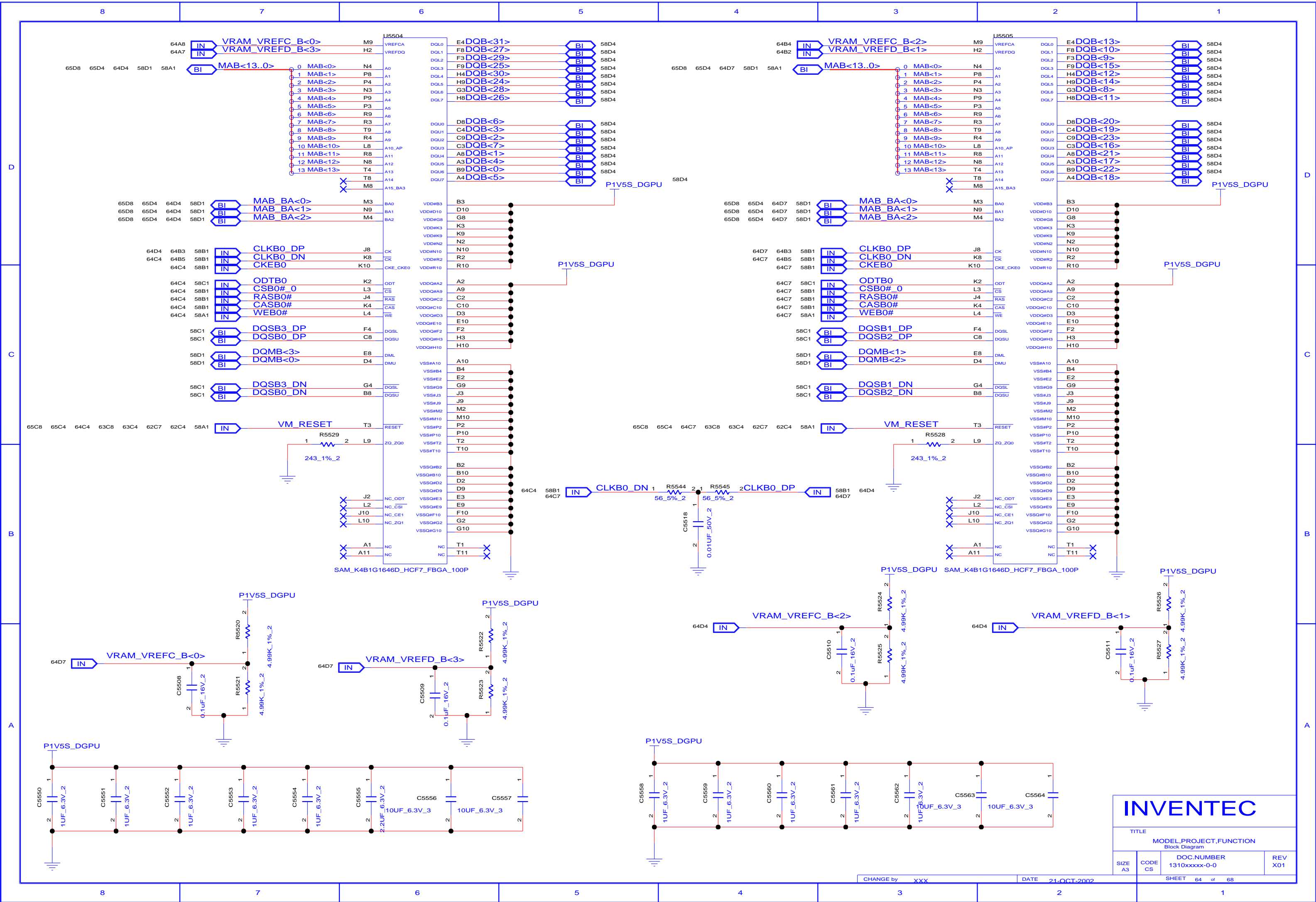
SIZE  
A3

CODE  
CS

DOC.NUMBER  
1310xxxx-0-0

REV  
X01

CHANGE by	XXX	DATE	21-OCT-2002	SHEET	63	of	68
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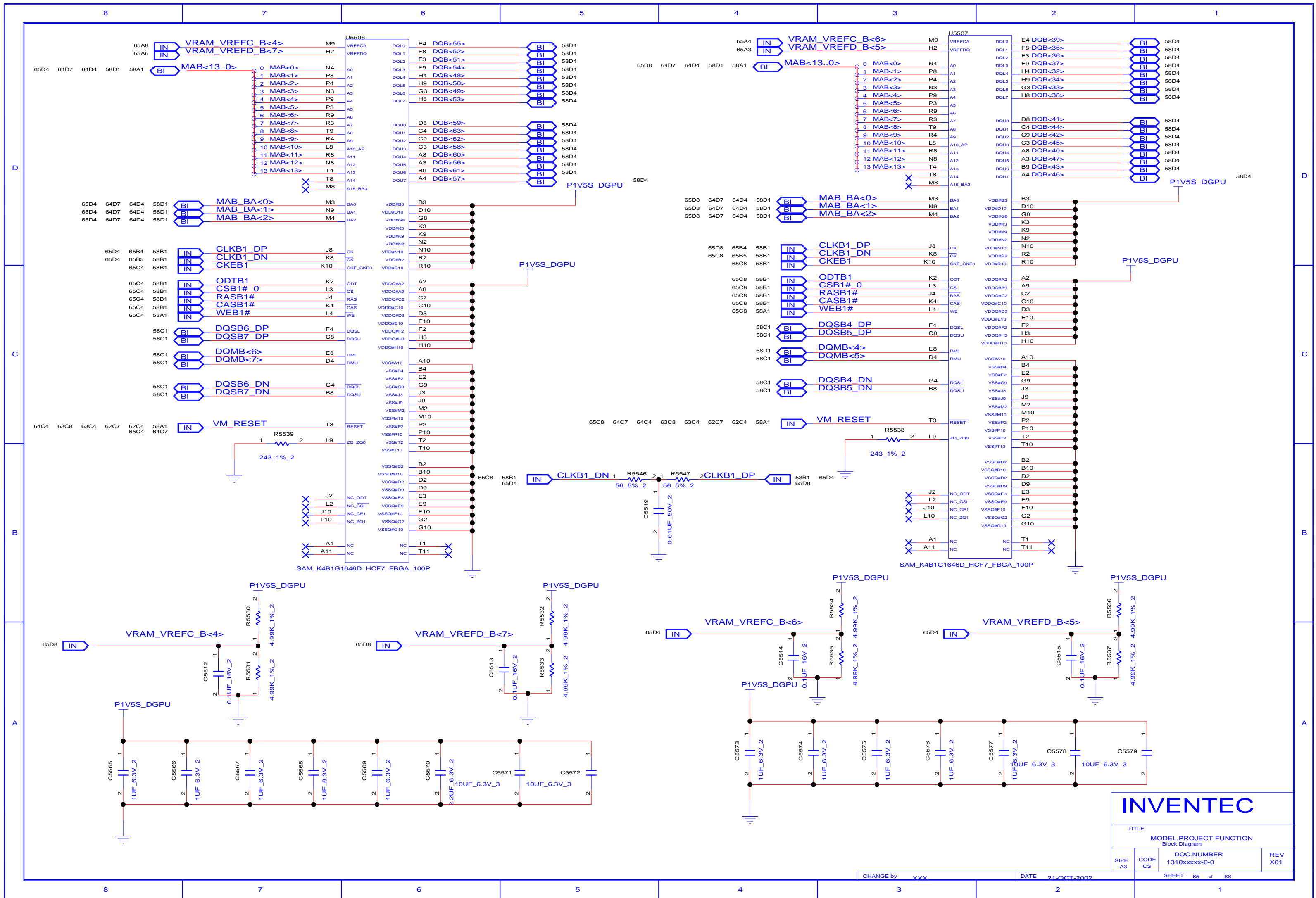
INVENTEC

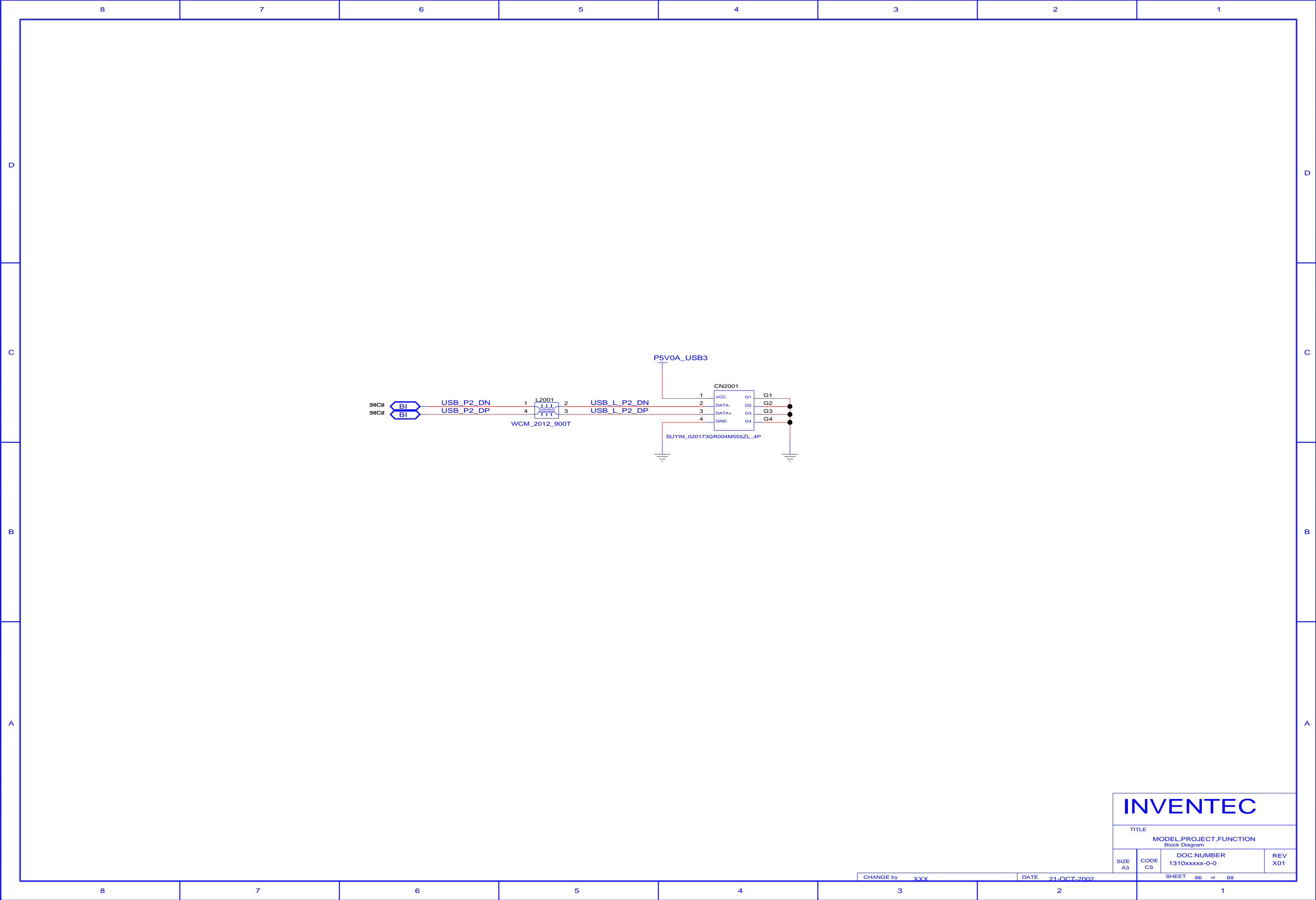
TITLE  
MODEL,PROJECT,FUNCTION  
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

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INVENTEC

TITLE

MODEL,PROJECT,FUNCTION

Block Diagram

SIZE A3

CODE CS

DOC.NUMBER 1310xxxxx-0-0

REV X01

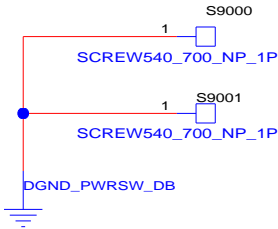
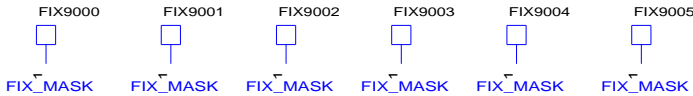
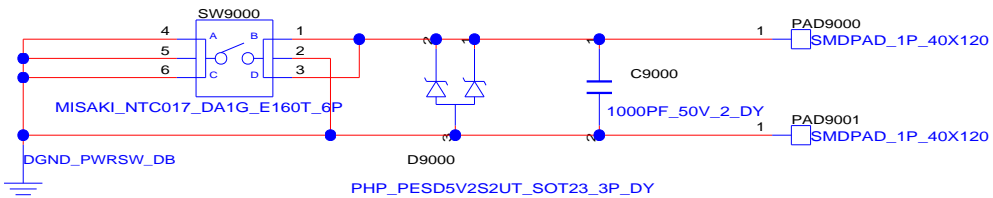
CHANGE by XXX

DATE 21-OCT-2002

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REFERENCE 9000~9999(SMALL BOARD)

POWER BUTTON



INVENTEC			
TITLE MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 67 of 68